Field Programmable Mixed-Signal Arrays (FPMA) Using Versatile Current/Voltage Conveyor Structures

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Abstract. Field Programmable Mixed-Signal Arrays (FPAA) designs are reviewed and standard building blocks described with respect to circuit parameters and design limitations. The second-generation current conveyor is introduced as an analog building block with properties similar to those of an operational amplifier, and which has the potential for high frequency operation. A current conveyor can be implemented in an area similar to that of a simple operational amplifier. Potentially greater bandwidths are achieved, while using CMOS technology instead of bipolar technology and test circuit design is proposed.

Keywords: Field Programmable Analog Array, Field Programmable Mixed-Signals Array, Programmable Universal Current Conveyor.

1 Introduction

FPAA designs are used in continuous-time or discrete-time modes. Discrete-time designs are programmed in terms of capacitor ratios but have limitations of lower bandwidths. Continuous-time circuits extend operating range to higher bandwidths, and offer no need of input/output anti-aliasing filters for applications in real-time signal processing, but they usually have higher distortion and require complex programming.

Published FPAAs designed at the building block level have used op-amps as their basic active element. For higher frequency bandwidths they could potentially be obtained by specifying higher power dissipation. However, in order to obtain significant gain from a simple op-amp-based amplifier, a designer must settle for significantly lower frequencies.

There are three potential options. The first would be to design an op-amp with greater frequency response. However, such an op-amp would occupy much greater die area and consume more supplying power. A second option would be to use a programmable compensation capacitor [1], where op-amp bandwidth can be extended if a high gain is desired. A third option is to use a block different than the operational amplifier, of which one possibility is the second-generation current conveyor [2].

2 Filed Programmable Analog Array Designs

A field-programmable analog array is an integrated circuit, which can be configured to implement analog functions using a set of configurable analog blocks (CAB) and a programmable interconnection network [3], and is programmed using on-chip memories.

An early conceptual FPAA design by Sivilotti [4] consists of CABs designed at the transistor level, and the interconnection network is based on a tree structure. Its target application was for the prototyping of analog neural networks. A fully-differential continuous-time CMOS design based on operational amplifiers and a modification to the Czarnul four MOSFET transconductors [5]. Its target application is for signal processing applications in the audio range, IC test results were presented for biquad filter, squaring, rectifier and VCO circuits. The CAB contains an op-amp and switchable feedback capacitors, and can also be used to implement a comparator by turning off the compensation capacitor.

Zetex Semiconductors Ltd. has introduced the Totally Reconfigurable Analog Circuit TRAC which includes 20 CABs, organized in two rows of 10 CABs, each capable of implementing one of the eight following functions: log, anti-log, non-inverting pass, addition, negating pass, op-amp, half-wave rectification, and off. Topological programming is implemented by turning CABs off, and by external wiring of the pins. Architecture is shown in Fig. 1.

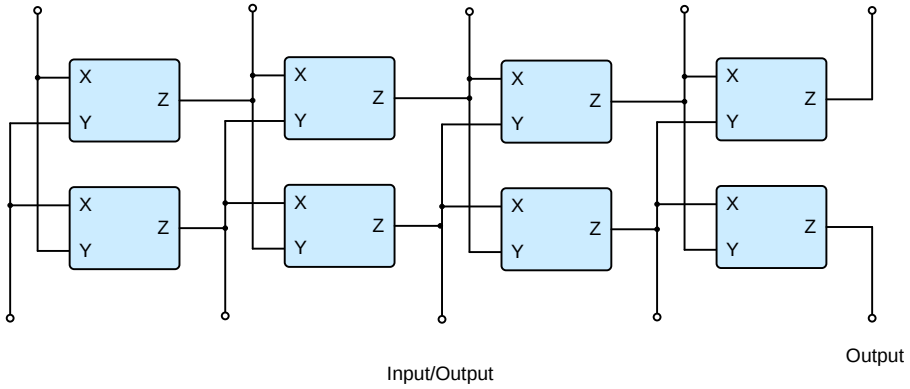

Fig. 1. TRAC Array Architecture

3 Configurable analog block

CAB (Configurable Analog Block) is used in an FPAA design as a principal block. Functions of a CAB include comparison, differentiation, amplification, integration, addition, subtraction, multiplication, log, anti-log. Current conveyor based implementation of basic CAB is shown in Fig. 2. Circuit is capable to realize amplification, first-order filtering functions, and with supplemented switchable diodes on the X and Z nodes log and anti-log functions could be realized, too.

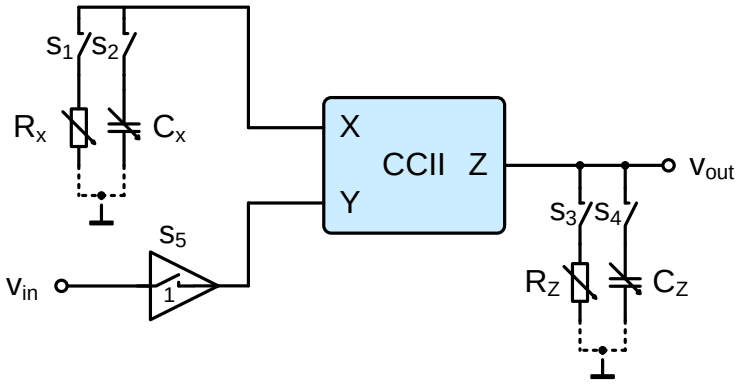

Fig. 2. Configurable Analog Block

The CAB consists of a second generation current conveyor, two transconductors, two programmable capacitors, and a buffer. Programmable resistors are realized with the transconductors. The function of the CAB is described in Tab. 1.

Table 1. Realization of CAB function with second generation current conveyor

Function	Configurable Analog Block				
	S1	S2	S3	S4	S5
Amplifier	1	0	1	0	1
Integrator	1	0	0	1	1
Lossy integrator	1	1	1	1	0

4 Programmable Universal Current Conveyor – PUCC

Programmable Universal Current Conveyor (PUUC) is a special type of the Universal Current Conveyor (UCC) [6] developed for FPAA. The idea is depicted in Fig. 3.

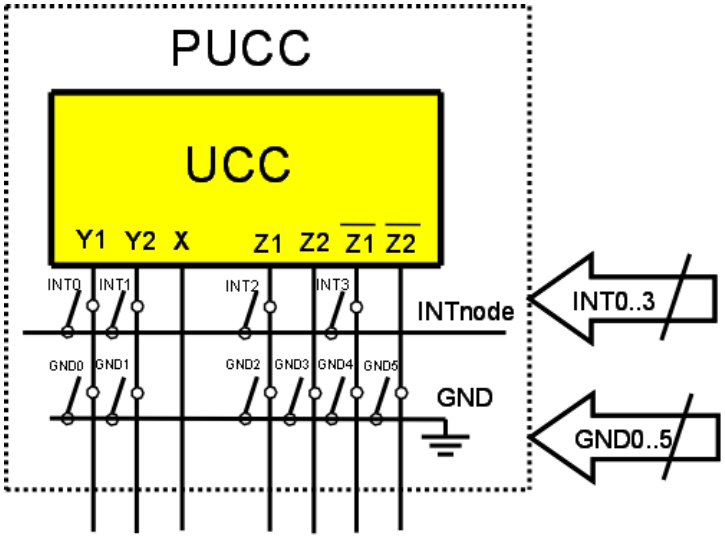

Fig. 3. Universal Current Conveyor

PUCC uses a standard UCC with 8 switches controlled by 2 independent buses (4b INT bus, 6b GND bus). It is possible to reconfigure UCC into 18 different simple current conveyors (with only one Y input) using these buses (Tab. 2). Moreover, the UCC structure offers current conveyors with fully differential voltage input. When using UCC (PUCC), the current conveyors with differential input could be use in very simple way.

Table 2. Reconfiguration of UCC

PUCC	INT BUS (4b)						GND BUS (6b)					
	Y1	Y2	Z1	Z2	notZ1	notZ2	Y1	Y2	Z1	Z2	notZ1	notZ2
CC type	INT0	INT1	INT2		INT3		GND0	GND1	GND2	GND3	GND4	GND5
CCI-	1	0	1		0		0	1	0	1	0	1
CCI+	1	0	1		0		0	1	0	0	1	1
CCI+/-	1	0	1		0		0	1	0	0	0	1
CCII-	0	0	0		0		0	1	1	1	0	1
CCII+	0	0	0		0		0	1	0	1	1	1
CCII+/-	0	0	0		0		0	1	0	1	0	1
CCIII-	1	0	0		1		0	1	1	1	0	0
CCIII+	1	0	0		1		0	1	0	1	0	1
CCIII+/-	1	0	0		1		0	1	0	1	0	0
ICCI-	0	1	1	0	0	0	1	0	0	1	0	1
ICCI+	0	1	1	0	0	0	1	0	0	0	1	1
ICCI+/-	0	1	1	0	0	0	1	0	0	0	0	1
ICCII-	0	0	0	0	0	0	1	0	1	1	0	1
ICCII+	0	0	0	0	0	0	1	0	0	1	1	1
ICCII+/-	0	0	0	0	0	0	1	0	0	1	0	1
ICCIII-	0	1	0	0	1	0	1	0	1	1	0	0
ICCIII+	0	1	0	0	1	0	1	0	0	1	0	1
ICCIII+/-	0	1	0	0	1	0	1	0	0	1	0	0

The proposed FPAA test chip structure is shown in Fig. 5. The FPAA structure (consists of 4 CABs) on the right side is similar to architecture of TRAC device [7]. The structure uses PUCC is on the left side. Test chip offers the possibility of architecture comparison. The PUCC structure promises huge versatility, but on the other hand the complexity of the PUCC block are probably the disadvantage if it is compared with simple CCII structure (more parasitics from switches, more control logic). Next chapter presents a current conveyor-based FPAA architecture.

5 Current Conveyor Implementation of the Zetex TRAC

Previously introduced Zetex TRAC is a bipolar design achieving 4 MHz bandwidth. Its noteworthy feature is the absence of switches in the signal paths, resulting from the hardwired interconnection network. This can boost performance by limiting the parasitics in the routing and can result in greater linearity.

A CMOS CCU-based TRAC design includes CABs which are arranged in a manner as depicted in Fig. 4.

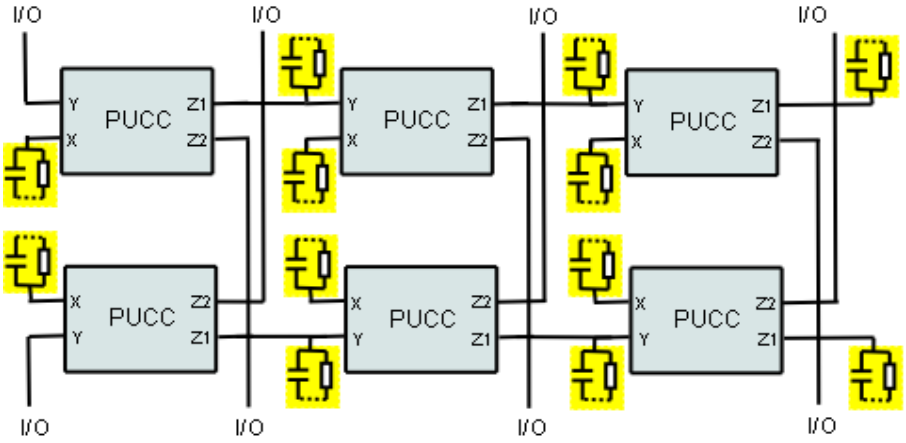

Fig. 4. Proposed FPPA TRAC based architecture using PUCC

Hardwired connections are used to route voltage signals between subsequent CABs. The leftmost pins act as inputs and the rightmost pins act as outputs. The intermediate pins can be configured both as inputs and outputs. To configure a pin as an input, the previous CAB whose output is connected to the pin, should be turned off. This is accomplished by turning off the CCII's bias currents, as shown in Fig. 4. This approach is similar to that proposed for the Praemont et al architecture [8], but could result in a significant waste of silicon area if too many CABs should be turned off.

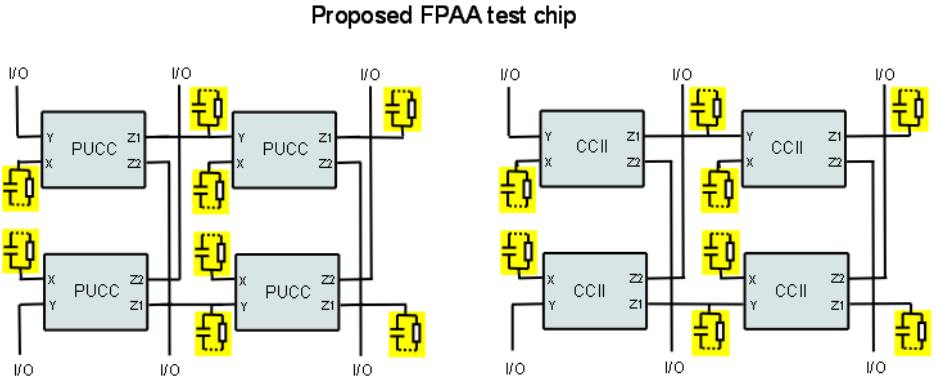

Fig. 5. Proposed test chip

6 Fully-Differential Implementation

All current conveyor blocks presented thus far have employed single-ended signaling. However, fully-differential signaling has advantages in terms of immunity to common-mode noise. A potential fully-differential current conveyor amplifier block is depicted in Fig. 6, and includes two CCII, and two resistors. Here the current I_x is equal to $(V_{in+}\text{-}V_{in-})/R_X$.

That current then flows across R_Z, producing an output $(V_{out+}\text{-}V_{out-})=(R_Z/R_X)(V_{in+}\text{-}V_{out-})$.

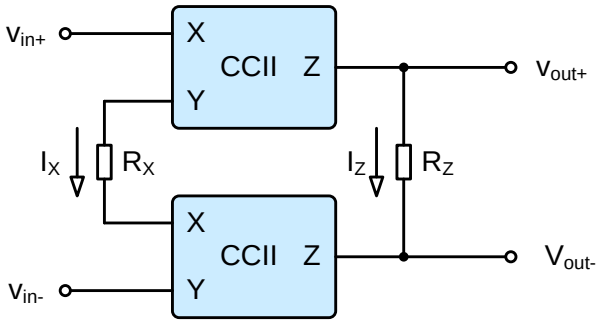

Fig. 6. Fully-Differential CCII Amplifier

7 Universal current conveyor

PUCC can be used as basic building block for design of Fully Differential Amplifier. Realized differential inputs are implemented in Universal Current Conveyor [6].

8 Filter design using FPAA

Suitable autonomous circuit was our starting point when designing the RC-active networks with current conveyors. For example, a simple circuit as shown in Fig. 7a could be chosen. It contains two general current conveyors, GCC, and five grounded passive one-port elements (resistors or capacitors) characterized by their admittances. The realization of this autonomous circuit using proposed FPAA is shown in Fig. 7b.

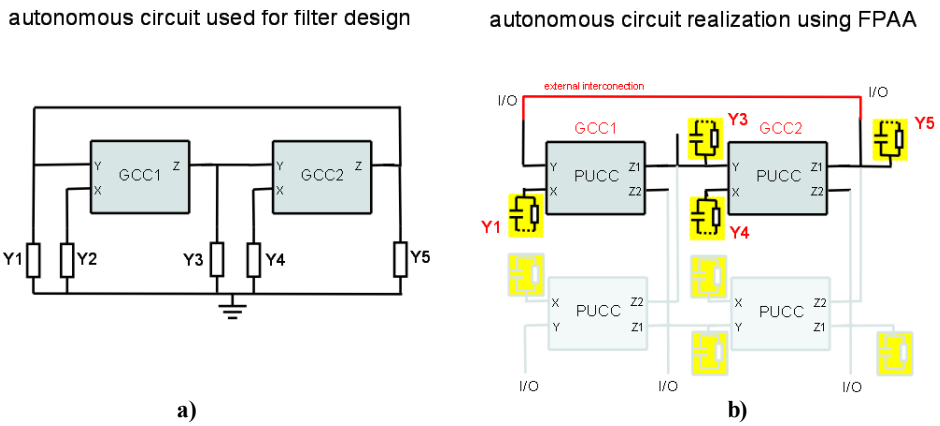

Fig. 7. Realization of filter using FPAA circuits

The universal filter design procedures using autonomous circuit (Fig. 7) were published in [9], [10], [11]. There was shown in those papers that this circuit works as multifunctional filter, moreover it could operate in both modes – voltage and current ones. Filter is determined by used types of current conveyor (instead of GCC1 and GCC2) and types of passive elements. Using proposed PUUC based FPAA for realizations of these filters brings huge versatility and design freedom for designers.

9 Summary

This paper has presented a design for a field-programmable analog array, with architecture similar to that of a commercially available FPAA. The advantage of the new method is that potentially greater bandwidths could be achieved, while using CMOS technology instead of bipolar one. Also, a fully-differential configurable analog block, which uses PUCC, has been presented.

10 Conclusion

A field-programmable analog array consists of configurable analog blocks, interconnections, as well as memories capable to configure the array into useful

analog circuits. FPAA circuits in the literature were reviewed and discussed obstacles in the development of a high-frequency FPAA. Among these main role was played by the low bandwidth of the simple operational amplifier.

The second-generation current conveyor was introduced, an analog building block with properties similar to those of an operational amplifier. It has the potential for higher frequency operation. A current conveyor can be implemented in an area similar to that of a simple operational amplifier. Also, reasons were stated as to why a current conveyor is preferable over a simple operational amplifier.

Low Power Supply Voltage

With the increase in the use of mixed-signal techniques, there will be compulsion to design analog circuits with lower power supply voltages. This is already evident in many deep submicron designs which use a single 3.3 V power supply (or even lower one) [12], [13], [14]. A current conveyor providing rail to rail swings at low power supplies should be developed.

Performance Limitations

Performance limitations of FPAAs were described. Some performance limitations included the speed of op-amps, transconductors, and comparators. By using current conveyors rather than simple op-amps, the performance of FPAAs could be increased to higher bandwidths. However, current conveyors as they stand, as well as existing transconductors, will not allow an extension of CMOS FPAAs to RF bandwidths. For that purpose, new architectures will need to be studied.

FPAA performance parameters other than bandwidth should be examined and improved upon, as well. Such parameters should include versatility and linearity.

Acknowledgement. This research has been supported by Ministry of Education of the Czech Republic in the frame of Research Program MSM0021630503 *MIKROSYN*, by the contract GAAV 1QS201710508, and by the FRVS 2353/2007 project.

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