Modeling and Design of a Novel Integrated Band-Pass Sigma-Delta Modulator

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Abstract. The paper deals with a bandpass sigma-delta modulator (BP SDM), which is used for conversion of signal from capacitive pressure sensor. This approach is absolutely new and unique, because this kind of modulator is utilized only for wireless and video applications. The main advantage of BP SDM is due to its defined band. That is why it is resistant against offsets of its sub-circuits. Another important advantage is low power consumption, since the BP SDM digitizes only narrow band instead of whole Nyquist band with similar dynamic range. The paper shows basic ideas of this approach and simulation results. The main stages are implemented in switched-capacitor (SC) technique. The paper presents two possibilities how to design PLL block. The first one is conventional approach and the other one is with digital sigma-delta modulator as generator of input harmonic signal.

Keywords: Band-pass sigma-delta modulator, capacitive pressure sensor, phase locked loop

1 Introduction

Band pass sigma-delta modulators (BP SDMs [1], [2], [3]) are well suited for direct conversion of the digitally modulated signals (QAM, PSK) from the frequency to the digital output. Once the RF signal is digitized, most of the signal processing tasks like channel filtering, demodulation etc. can be easily done in the digital domain with high degree of programmability. Induced noise and high sampling frequencies requires corresponding electronic technology as it is used in implementation for GPS/GSM communication systems.
The binary flow from the BP SDM output is down converted by digital multiplier and in the LP digital filter transformed in the digital number. The whole structure represents band pass sigma-delta analog to digital converter (BP SD ADC). Coherency between input signal fin and clock frequency ($f_s = 4f_{in}$) in the BP SD ADC makes converter phase sensitive.

Authors introduce a new application of BP SDM as the processing circuit from the capacitive pressure sensor with the direct digital outputs representing real and imaginary components of the input vector. The simple BP SDM first generation was designed for integrated sensor system using CMOS 07 technology. The defined narrow band is advantage against offsets of modulator sub circuits such as OPA, delay stage and summator. The modulator is tuned at 62.5 kHz sampling frequency. It processes the signal with central frequency f_c = 15 625 Hz. The paper shows comparison of proposed ideal and real BP SDM.

2 The BP SDM topology

Fig. 1 shows block diagram of BP SDM [4]. It contains band-pass filter (BPF), an N-bit quantizer and a digital to analog converter (DAC), which is connected in a loop. The BPF can be synthesized by cascading two or more second-order biquadrate filters or resonators, which must have a sharp transfer function and well-defined resonance at f_n. These resonators may be implemented as a discrete-time filter using either SC or SI techniques or they may be implemented as a continuous time filter.

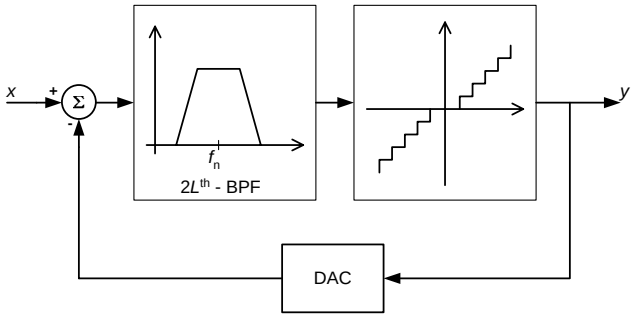

Fig. 1. Basic block diagram of a BP SDM

Let consider $2L^{th}$-order BPF composed of a cascade of L resonators with a DT transfer function given by

$$H_R(z) = \frac{1}{(1 - z^{-1} z_n)(1 - z^{-1} z_n^*)} \tag{1}$$

where z_n and z_n* are the conjugate-complex poles of $H_R(z)$.
The output of modulator in Z-domain, assuming quantization error is

$$Y(z) = S_{TF}(z) X(z) + N_{TF}(z) E_q(z) \tag{2}$$

The signal transfer function (*STF*) and noise transfer function (*NTF*) are as follows

$$S_{TF}(z) = \frac{\left[N_R(z)\right]^L}{\left[N_R(z) + (1 - z^{-1}z_n)(1 - z^{-1}z_n^*)\right]^L} \tag{3}$$

$$N_{TF}(z) = \frac{\left[(1 - z^{-1}z_n)(1 - z^{-1}z_n^*)\right]^L}{\left[N_R(z) + (1 - z^{-1}z_n)(1 - z^{-1}z_n^*)\right]^L} \tag{4}$$

The output transfer characteristics for the first generation BP SDM utilized for processing circuit is

$$Y(z) = X(z).z^2 + E_q(z)\left(1 + z^2\right) \tag{5}$$

Power density after noise shaping in the spectral domain is

$$\varepsilon_{NS}^2(f) = \varepsilon_q \frac{4}{f_S}\left(1 + \cos\frac{4\pi f}{f_S}\right) \tag{6}$$

The Fig. 2 shows the capacitive pressure sensor where one branch is sensing branch and another is reference branch.

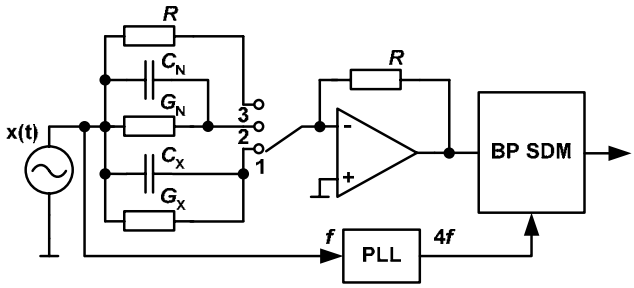

Fig. 2. Measurement chain with BP SDM

While the pressure influences the capacity ΔC_X the humidity impacts the conductivity ΔG_X of the sensing branch. Pre-processing circuit with BP SDM converts it after synchronized down-conversion into its real and imaginary part. The binary flows are converted into digital number in two digital low pass (D-LP) filters. The digital resolution is proportional to the time window of the D-LP filter. The BP SDM is

controlled coherently with the input source frequency. The digital output values are determined by the quantized vectors in all three switch positions as follows

$$\begin{aligned} U_1 &= RU\left[j\omega\left(C_N + \Delta C_X\right) + G_N + \Delta G_X\right] \\ U_2 &= RU\left[j\omega C_N + G_N\right] \\ U_3 &= RU \end{aligned} \tag{7}$$

The phase shift of the processing block is suppressed by the subtracting operation. The difference of the digital values from the output of the LP filter in the position 1 and 2 normalized to the value measured in the position 3 is expressed by the formula. Here measured changes of capacity and resistance are obtained

$$\frac{U_1 - U_2}{U_3} = R\left(j\omega\Delta C_X + \Delta G_X\right) \tag{8}$$

The BP SDM is tuned on 62,5 kHz of sampling frequency as mentioned, it means that central frequency is

$$f_c = \frac{f_s}{4} = \frac{62500}{4} = 15625\,Hz \tag{9}$$

Formula (6) shows the minimal value of the noise shaped power density around the central frequency f_c.

3 Design of auxiliary stages

This chapter describes the design procedure of generator of harmonic signal and phase locked loop (PLL).

3.1 Generator of input harmonic signal utilizing sigma-delta modulation

The digital design has been used for simplicity of chip realization. The sine wave signal is generated by means of digital sigma-delta modulation. The output from sigma-delta modulator is connected to analog low pass filter. The output sine wave signal is obtained after high frequency filtering. The input clock frequency of digital part is 4 MHz. This frequency is common for all digital stages. The digital part is proposed using VHDL language.
The whole system consists of four blocks as can be seen from Fig. 3.

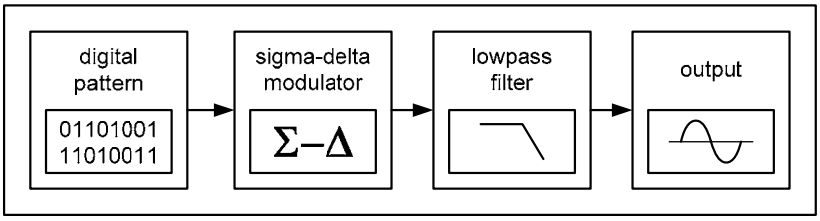

Fig. 3. Generator block diagram

Thanks to this condition, the design is very flexible and each part could be changed very easily. The first stage of this proposal is generator of digital image of output sine wave signal, which is described in VHDL language.

The core of the whole generator consists of sigma-delta modulator. The first order modulator is used for simplicity of design. The modulator (Fig. 4) includes summator and subtractor. The input and output signals are connected on it. The difference (sum) is connected to the register. The value in this register is increased at each clock pulse. The register output is compared in comparator zero reference value. In case when register value is higher than zero, the comparator reverse into logic high, in other cases is zero. The comparator output is modulated sine wave signal. It could be filtered and analog signal could be obtained. The output is directly connected to the analog low-pass filter.

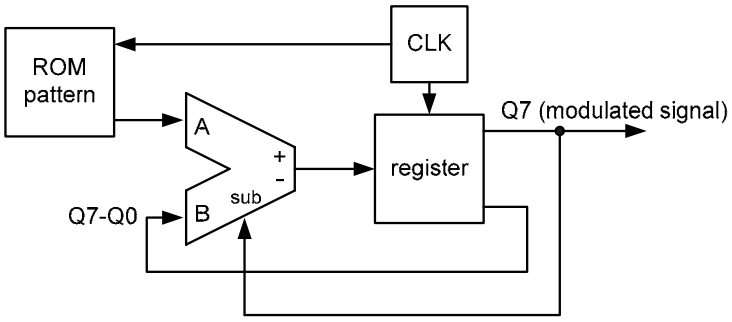

Fig. 4. The block diagram of sigma-delta modulator

The modulator realization is shown on Fig. 4. This whole part (from look-up memory ROM till output) is programmed in VHDL. The comparator has been replaced by MSB of register for simplicity, because the decision level of comparator has been set at binary number 64, which is zero reference value. Thanks to this modification, the design is sign-less.

The last stage is low-pass filter. It is only analog part of the whole proposal. This filter has been designed separately. It has been chosen third order active Butterworth RC filter with cut-off frequency of 15 625 Hz. The filter makes analog signal from modulated signal.

The digital stages have been designed in VHDL language in Xilinx ISE WebPack design environment. The simulation (Fig. 5) proceed in simulation program ModelSim Xilinx Edition. The main aim was to obtain as simple control logic as

possible because of chip area. The design has been tested and finalized in FPGA Spartan-3.

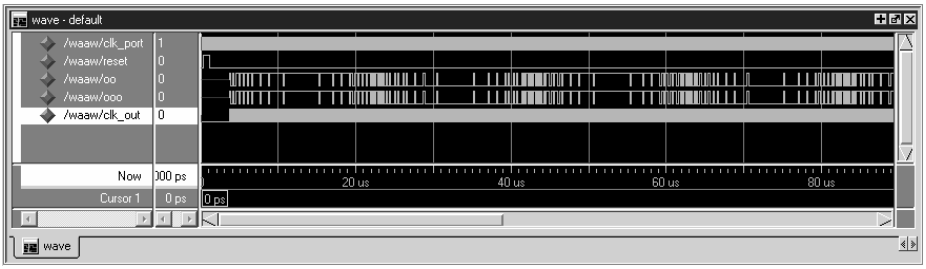

Fig. 5. The simulation of digital stage function

The analog part is low-pass filter. First the simple RC filter has been used and its function has been verified. Then the third order RC filter has been utilized with exact frequency of 15 625 Hz. The 4 MHz frequency of pulses at modulator output is obtained. Therefore this filter should be allowed to separate sine wave signal from digital noise at the output sufficiently. Filter consists of one fast OPA.

3.2 Design of PLL

The PLL stage is designed utilizing well-known structures, which is shown on Fig. 6. The input sinewave signal is converted by means of comparator onto pulses. Than phase detector, which is bipolar charge pump compares phase between these pulses and signal generated by VCO (Voltage Controlled Oscillator).

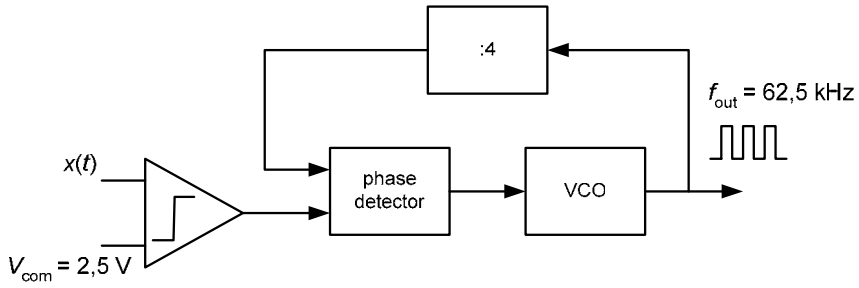

Fig. 6. Block diagram of designed PLL

The VCO is designed as starving ring oscillator with current controlled invertors as shown in Fig. 7.

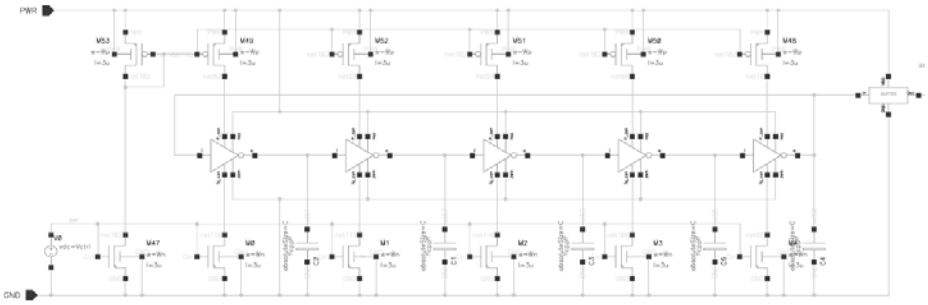

Fig. 7. Schematic diagram of VCO

The VCO is designed for 25 μA driving current at control voltage 1.3 V. The ring oscillator consists of 5 controlled invertors. Since the output frequency has to be very low, there are used capacitors to produce the time delay.

The phase detector (PD) detects the phase difference between the reference signal and the feedback signal from the VCO and frequency divider. Note that, although the PD of a PLL can be an analog multiplier, an exclusive-or (XOR) gate or a J-K flip-flop, etc, for a frequency synthesizer we always use the charge-pump PLL with a tri-state phase-frequency detector (PFD) that also detects frequency errors.

4 Modeling of PLL with generator of input harmonic signal

The PLL with generator of harmonic signal utilizing sigma-delta modulation was designed and simulated in MATLAB SIMULINK and ModelSim. Model of generator of input harmonic signal and additional synchronizing digital logic are described in VHDL language. Output signal of generator is filtered by low pass filter. This filtered signal is led to comparator. Comparator output is feedback signal to VHDL model of generator. This feedback signal is represented as synchronization signal. Proposed model of PLL with generator of harmonic signal utilizing sigma-delta modulation is shown in Fig. 8.

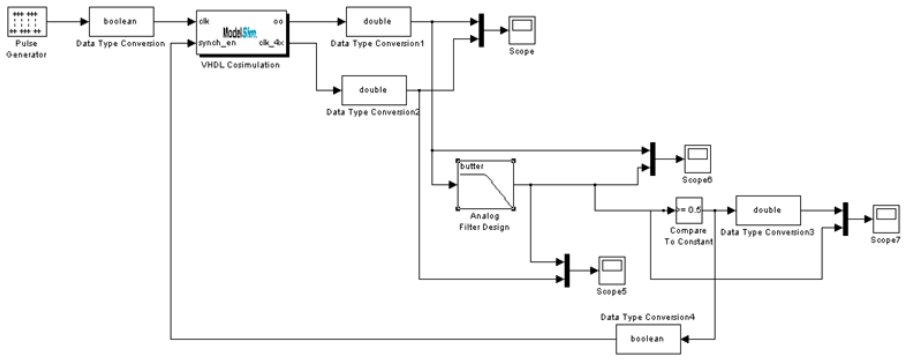

Fig. 8. Model of PLL with generator of input harmonic signal utilizing sigma-delta modulation

Matlab simulation results of PLL with generator of harmonic signal utilizing sigma-delta modulation is shown on Fig. 9. Modelsim simulation results of PLL with generator of harmonic signal utilizing sigma-delta modulation is shown on fig. 10.

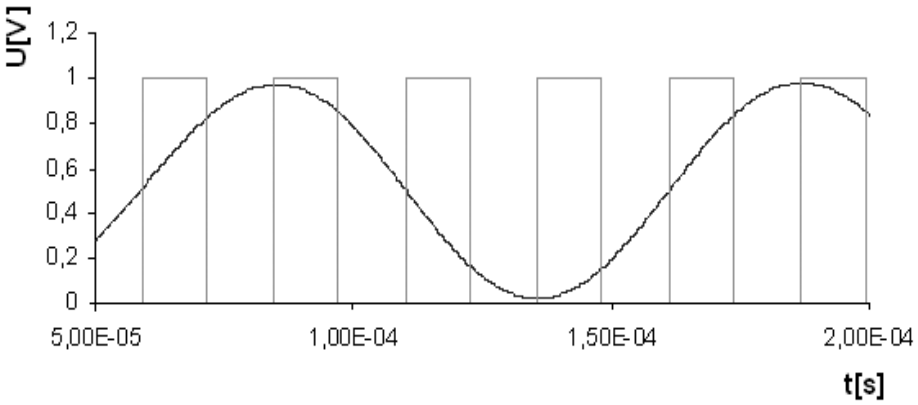

Fig. 9. Matlab simulation results of PLL with generator of harmonic signal utilizing sigma-delta modulation

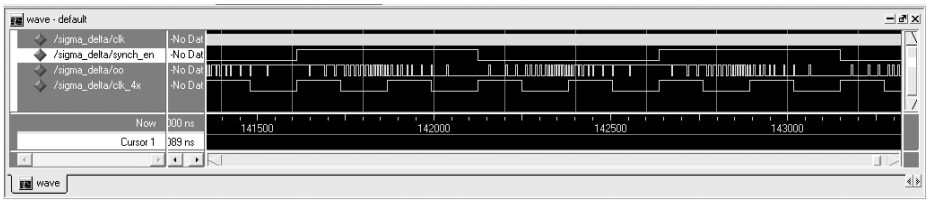

Fig. 10. ModelSim simulation results of PLL with generator of harmonic signal utilizing sigma-delta modulation

5 Design of band-pass modulator in Cadence

The switching of the inputs is synchronized with internal switching of modulator since it uses blocks with SC technique.
The ideal BP SDM consists of input S/H circuit, summator, four delay circuits, comparator and DAC connected in closed loop. There are several addition stages mainly D flip-flop and XOR logic gate. These stages are utilized to satisfy clock synchronization with driving clock. It is important to note that ideal BP SDM uses ideal OPAs (voltage controlled voltage source with very high gain), ideal capacitors and it has no offsets, noise sources etc.
The behavior of modulator has been simulated with input signal frequency 15625 Hz with sweeped amplitude from 0 to 1 V. The computed values are average values of logic 1 and logic 0 (represented as 5 V and 0 V respectively). It means that number on y axis is ratio between logic levels appropriate to input amplitude. The most important output is XOR output.
It can be seen that this output is quite linear and appropriate to input amplitude. The beginning of the curves is affected by start-up phase of modulator and should not be considered. The real BP SDM circuitry is depicted on Fig. 11.

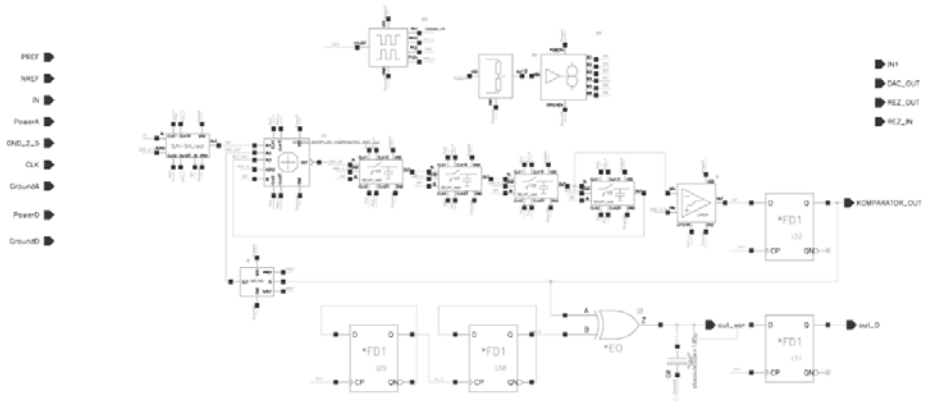

Fig. 11. Block diagram of real BP SDM

The delay and S/H circuits are designed in SC technique. Comparator is proposed with latch. The DAC is simple 1-bit circuit. This modulator has been designed and simulated in Cadence software using CMOS 07 technology. The power supply is 5 V. The systematic offset of the basic loop is 140 μV.
Since this is the first realization of that kind of chip for capacitive pressure sensors, there are many auxiliary pins used for testing measurement. The aim of this arrangement is to obtain maximum information about behaviour of each stage of BP SDM. The most critical parts are blocks using switched-capacitor approach, because there are many nonidealities and error sources, mainly clock feedthrough and noise. Table I. lists all pins, which will be led out of the chip for testing.

Tab. 1. Expected list of pins for 24-DIL package

Pin no.	Name	Description	Function
1		not used	
2	VSS	input	supply of digital part
3	VSSA	input	supply of analog part
4	VDDA	input	supply of analog part
5	OUT_SH	output	output of S/H circuit
6	IN	input	analog input
7	REZ_IN	output	output of summator
8	DAC_OUT	output	output of DAC
9		not used	
10	REZ_OUT	output	output of delay circuits
11	AGND	input	analog ground
12	NREF	input	negative reference voltage of DAC
13		not used	
14	PREF	input	positive reference voltage of DAC
15	PH2_n	output	output of nonoverlapping clock PH2_n
16	PH2	output	output of nonoverlapping clock PH2
17	PH1_n	output	output of nonoverlapping clock PH1_n
18	PH1	output	output of nonoverlapping clock PH1
19	OUT_D	output	output of D flip-flop
20	OUT_XOR	output	output of XOR (most important)
21		not used	
22	CLK	input	input of X-tal clock
23	KOMP_OUT	output	output of comparator
24	VDD	input	supply of digital part

The average outputs of real BP SDM depending on magnitude of analog input signal (range from 0 to 1 V) are shown on Fig. 12. It can be seen, that output of XOR is mostly linear, which is expected result.
Consequently the output plots of real BP SDM correspond with ideal one, so the proposed 1st generation BP SDM for pressure sensing works correctly.

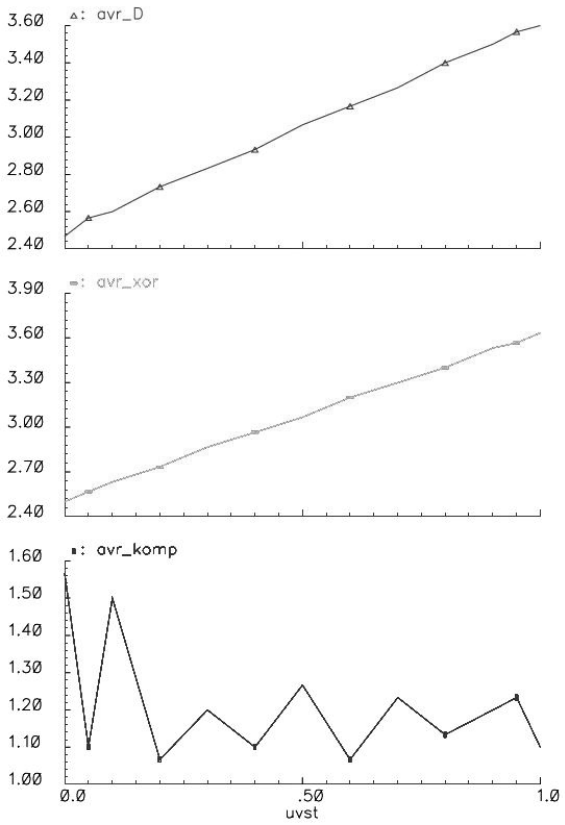

Fig. 12. Output plots of real BP SDM

6 Conclusions

The BP SDMs are well suited for wireless applications. This paper shows another way how to use its advantages. Authors designed 1st generation BP SDM as preprocessing block for capacitive pressure sensing. The behavior of real modulator has been verified and compared. Two possibilities of PLL design are presented in this paper. Both solutions will be designed on ASIC. The first one is conventional approach which is shown on fig. 6. The second one uses digital sigma-delta modulator as generator of input harmonic signal. This part with additional synchronizing digital logic is described by VHDL language. This digital part will be implemented on chip by using Synthesis and Place&Route tools. Matlab modeling of PLL with digital sigma-delta modulator is presented in this paper. Moreover, the test results will serve

to the chip redesign targeted on the improvement of the conversion accuracy and the reduction of the power consumption.

Acknowledgments

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