A High Speed Analog to Digital Converter for Ultra Wide Band Applications

Anand Mohan, Aladin Zayegh, Alex Stojcevski

Centre for Telecommunications and Microelectronics
School of Electrical Engineering
Victoria University
P.O. Box 14428
Victoria 8001, Australia
anand.mohan@research.vu.edu.au

Abstract. Over the past few years Ultra Wide Band (UWB) technology has taken the realms of communications circuit design to new levels. This paper demonstrates the design and simulation of a very high speed Flash Analog to Digital Converter (ADC) for UWB applications. The ADC was implemented in 90 nanometre (nm) CMOS design process. The converter works at an optimal sampling rate of 4.1 Gig-Samples per second (Gsps) for an 800 MHz input bandwidth corresponding to a 1V full scale reference. The converter has moderate linearity error tolerance of about ±1 LSB (62.5 mV) without use of any averaging techniques. The ADC works on a 1V supply and has an overall power consumption of 114 mW.

Keywords: ADC, UWB, CMOS Technology, Flash Topology, Power Saving

1 Introduction

The deregulation of the UWB frequency spectrum by the Federal Communications Commission (FCC) and subsequently by other countries has offered a tremendous boost to communications and applications that require a medium to transfer large amounts of data in a very short period of time. UWB offers an unparalleled medium for such high speed communications, with an effective transmitting bandwidth of almost 7.5 GHz. This means that data transmission in the range of few tens to hundreds of gigabits per second are now realisable. UWB transmission consists of signals that are in the form of sub-nanosecond pulses and are therefore transmitted and received at short distances but over a very large frequency range. Applications for UWB range from commercial high speed wireless access to very high data rate medical imaging systems. Typical UWB systems are characterized as having a signal bandwidth of 528 MHz or more. UWB offers advantages in its ability to resist multipath fading and jamming from nearby nodes, low spectral density and a very high channel capacity [1], [2].

The application of Shannon's Channel Capacity equation highlights the unique ability that UWB offers. The equation defines a unique relationship between the maximum data rate and the total transmission bandwidth, as seen in Equation 1.

$$Cx = fx * log\left[\frac{Pr}{Nt * fx}\right] \quad (1)$$

where C_x corresponds to the channel capacity, f_x is the channel bandwidth, N_t is the power spectral density of noise and P_r if the received power into the system [3].

The ADC being the heart of the system provides a unique challenge in its design for such high speed requirement. Section 2 details out UWB receiver and its characteristics. Section 3 details out he high speed ADC architecture, while section 4 gives an overview of obtained results.

2 UWB Receiver

Typically ideal UWB systems consist of a receiver chain with minimal components as illustrated in Fig. 1. The receiver front-end consists of a very large bandwidth Low Noise Amplifier (LNA), Variable Automatic Gain Control Amplifier (VGA) and Very High Speed ADC. The advantage that this architecture offers is a reduction in the total number of components in the front-end and an overall saving in power.

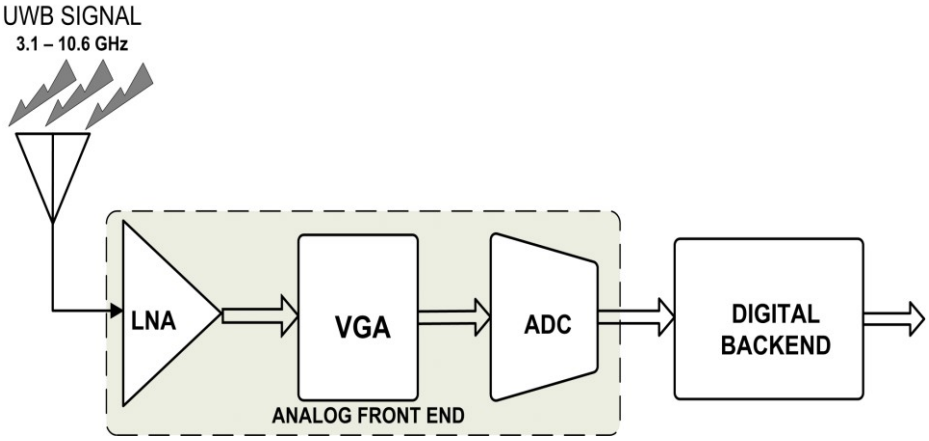

Fig. 1. Ideal UWB Receiver

For such a setup to be implementable would require a LNA to handle frequencies from 3.1 GHz to 10 GHz, VGA to provide amplification and stabilisation from about

-25 dBm to 0 dBm and an ADC to operate full scale at a minimum sampling frequency of 7 Gsps. This type of specification range will require CMOS systems to switch and thereby adjust to changing frequency ranges in a matter of few of picoseconds. For an ADC to effectively sample (Nyquist Rate) a 4 GHz input signal will require to have a clock with switching speed of 125 picoseconds. The fastest Flash converters [4] require all comparators to switch and work in perfect synchronisation. For low resolution converters the numbers of comparators are minimal, however in presence of mismatch and linearity problems, will require converters to have larger resolutions. Moreover with flash converters a single bit increase in resolution leads to a doubling in power consumption and thereby requiring preamplifier input bandwidth of more than 200 GHz. Present CMOS technology cannot switch efficiently at such high speeds without encountering mismatch and large scale linearity problems [4].

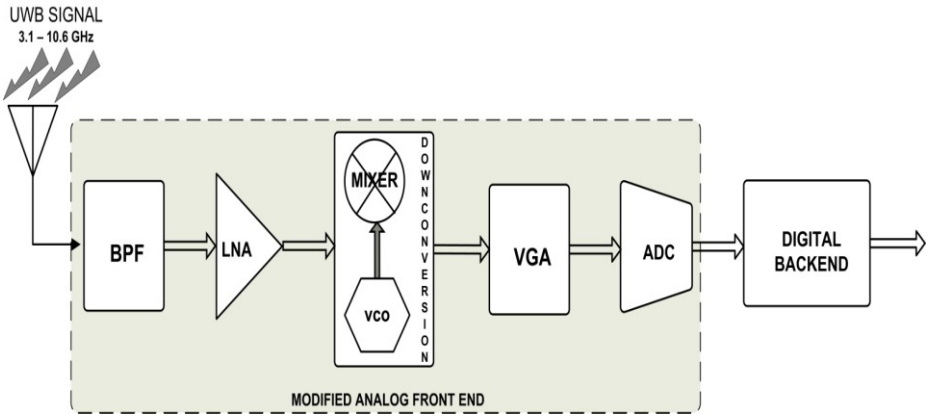

Fig. 2. Down-converted UWB Receiver

A more realistic approach is illustrated in Fig.2. A down conversion stage comprising of a mixer and a Voltage Controlled Oscillator (VCO) is used to reduce the frequency range to hundreds of megahertz to a few gigahertz. This intermediary setup relaxes the requirements on the ADC such that a very high speed digitiser can be realised in CMOS effectively [4], [5].

3 ADC Architecture

This section details out the design of the ADC for use in UWB systems. From [6] it can be estimated that for a Gaussian 5^{th} order down-converted frequency spectrum, having a effective bandwidth of 600MHz or more and residing in a frequency range of 1.3 GHz to 2.5 GHz, an over-sampled converter working at 4 Gsps is more than sufficient. Based on calculations in [5-7] it is seen that 4 bits are the optimum resolution to ensure reliable detection. A number of ADC architectures were looked

into and analysed comprehensively [8]. It is seen that among all architectures Flash based architecture is the most suitable choice for implementation. The parallel nature of Flash ADC with its array of synchronised comparators provides the fastest solution for UWB implementation [9-11].

The entire structure of the designed ADC is shown in Fig.3. It consists of a differential resistor ladder that provides full scale reference for all the comparators. A flash architecture consists of 2^X - 1 comparators for X bits, hence the ADC in this work consists of 15 comparators. Section 3.1 details the design of the high speed fully differential comparator and section 3.2 details out the design of a high speed MOS Common Mode Logic (MCML) Encoder.

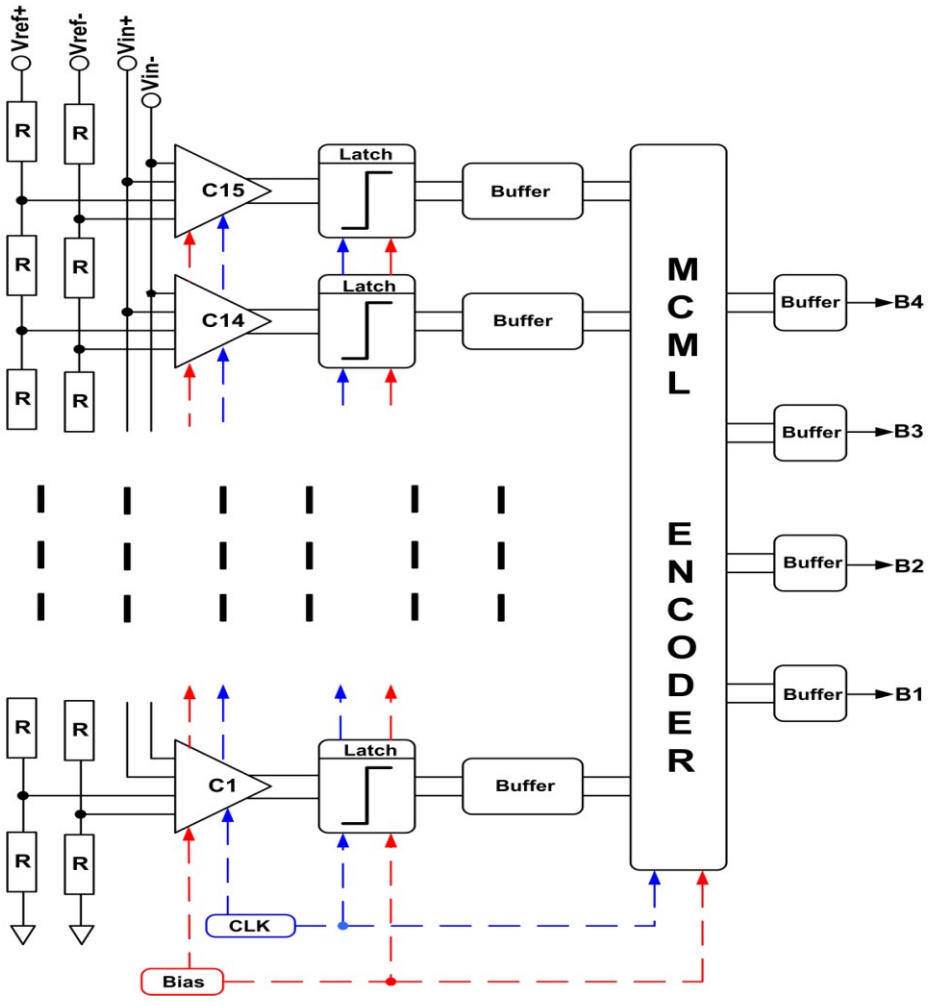

Fig. 3. ADC Architecture

3.1 Comparator Design

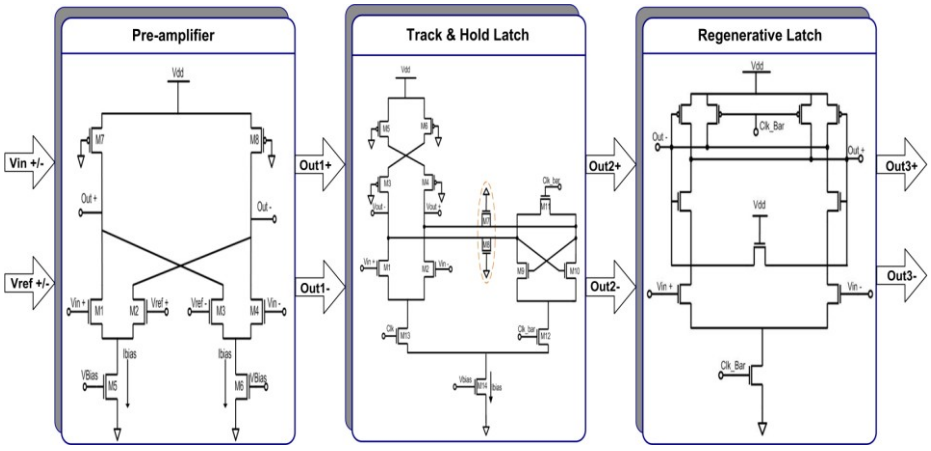

Fig. 4. Comparator

The comparator depicted in Fig. 4. is a low voltage fully differential three stage design. The first stage consists of an input pre-amplifier and two consecutive latches. The first latch is a differential track and hold latch while the second is a high speed regenerative latch.

Input Pre-amplifier. The pre-amplifier as shown in Fig.4. is a fully differential open loop architecture. This architecture provides many advantages over closed loop structures due to its high speed, low swing and low gain. The open loop structure also offers reduced power consumption and better rejection of V_{DD} noise. The pre-amplifier has an intrinsic gain defined by (g_m/g_{ds}), keeping in mind its low gain nature. Close to minimum length transistors are used for all the input differential pairs to ensure that there are reduced offset problems and ensure faster switching. The pre-amplifier is loaded with triode loads. This type of loading helps to keep the output slew rate to a minimum and also offers required voltage headroom. The input referred offset of the pre-amplifier was estimated based on Equation 2.

$$V_{os} = \left[\frac{\Delta L_{N-i}}{L_{N-i}} + \ldots + \frac{\Delta L_i}{L_i} + \frac{\Delta W_{N-i}}{L W_i} + \ldots + \frac{\Delta W_i}{W_i} \right] + V_T \qquad \textbf{(2)}$$

where V_{os} is the offset voltage, L_{N-i} is the length of the transistors change and W_{N-I} is the width of the transistor change for the input pairs [12], [13].

Track and Hold Latch. The latch is shown in Fig.4. It provides very low swing and very high speed operation. The latch is based on a clocking scheme such that

whenever the clock is high the input pairs are active and track in the input from the pre-amplifier. When the clock goes low the latch provides slight positive feedback and amplification. Like the pre-amplifier the latch also uses a cascaded cross coupled triode load that helps in the low swing operation. This loading scheme has advantage in that it helps to reduce the V_{DD} noise variation on the input pairs. The output settling time was optimised by setting the common mode voltage (V_{CM}) of the latch, as shown in Equation 3 [12], [13]. This type of latch has good slew rate and also provides sufficient tolerance to meta-stability problems [14].

$$V_{CM} = \frac{V_{DD}}{2} \tag{3}$$

Regenerative Latch. The final stage of the comparator is a regenerative latch (Fig. 4.) based on [13], [14]. The latch is used primarily to pull the output to logic rail to rail levels. The working of the latch is based on a clock that switches on the input pairs when the clock is high. When the clock is low it provides feedback and pre-charges the output to V_{DD}. The latch is self-biased and therefore offers a great saving in power consumption. The latch is sized to provide the required output swing. The output capacitances provide slightly different discharging times to enable proper feedback [13], [14].

3.2 Encoder

Fig. 5. shows the schematic of a high speed encoder. The encoder was based on a thermometer to binary conversion with an intermediate gray code stage. The gray code stage provides only a 1 bit transition between consecutive states and thereby reduces the effects of code skipping and bubble errors at the output of the encoder. The encoder is designed used MOS Common Mode Logic (MCML). This type of design is the most efficient in terms of speed and very low swing signal operation. The encoder was designed such that the 15 outputs from the comparators are fed through a series of NAND/AND gates such that they are converted to 4 bit gray code and then re-converted from 4 bit gray code to a 4 bit binary output [15].

The design equations for the implementation of the encoder are highlighted below. A set of equations (Equation 4.) shows the conversion from thermometer to gray code and another set of equations (Equation 5.) shows the succeeding conversion from gray to 4 bit binary.

Thermometer to Gray Code Conversion:

$$\begin{aligned} K1 &= \overline{C1\overline{C3}} \bullet \overline{C5\overline{C7}} \bullet \overline{C9\overline{C11}} \bullet \overline{C13\overline{C15}} \\ K2 &= \overline{C2\overline{C6}} \bullet \overline{C10\overline{C14}} \\ K3 &= C4\overline{C12} \\ K4 &= C8 \end{aligned} \tag{4}$$

Gray to Binary Code Conversion:

$$
\begin{aligned}
B1 &= K1 \oplus B2 \\
B2 &= K2 \oplus B3 \\
B3 &= K3 \oplus B4 \\
B4 &= K4
\end{aligned}
\tag{5}
$$

The output of the encoder is then buffered to get a sharp switching response with minimal rise and fall times.

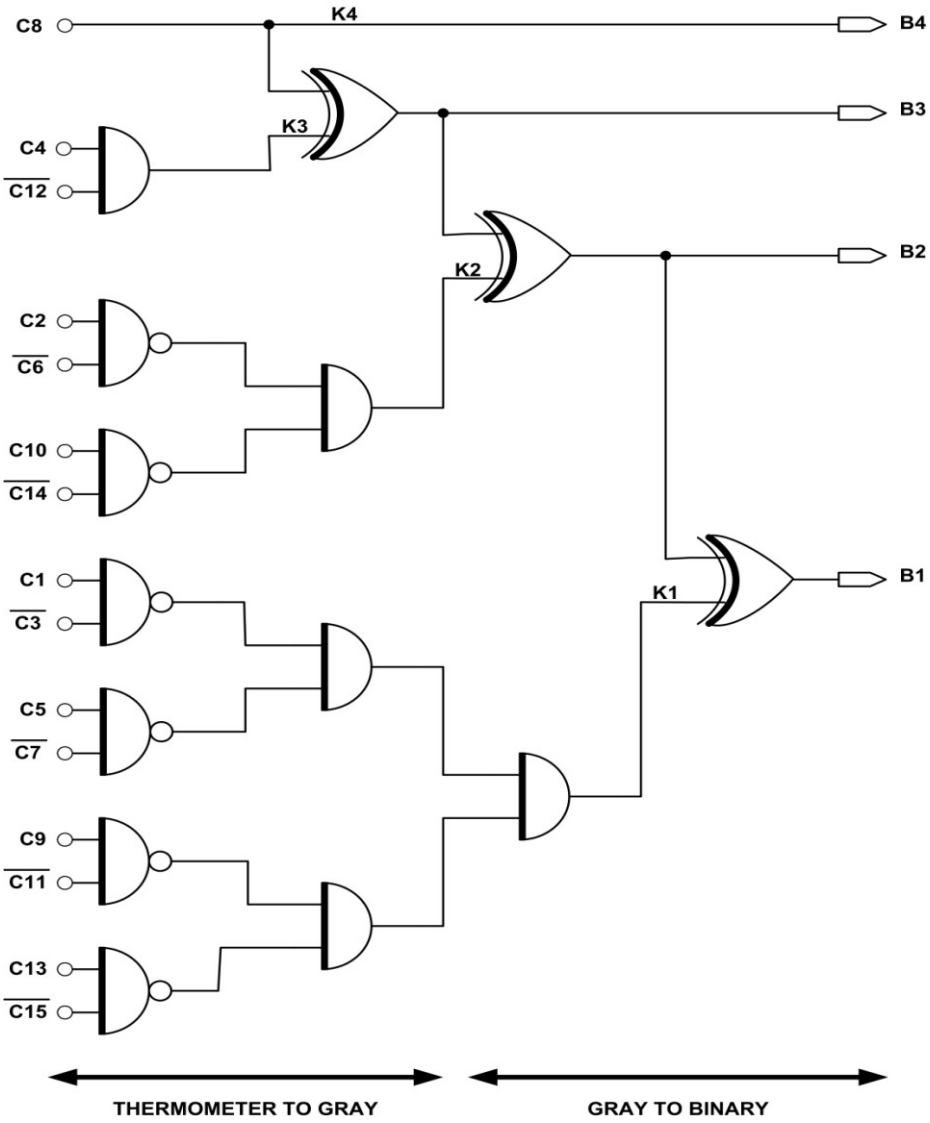

Fig. 5. Encoder

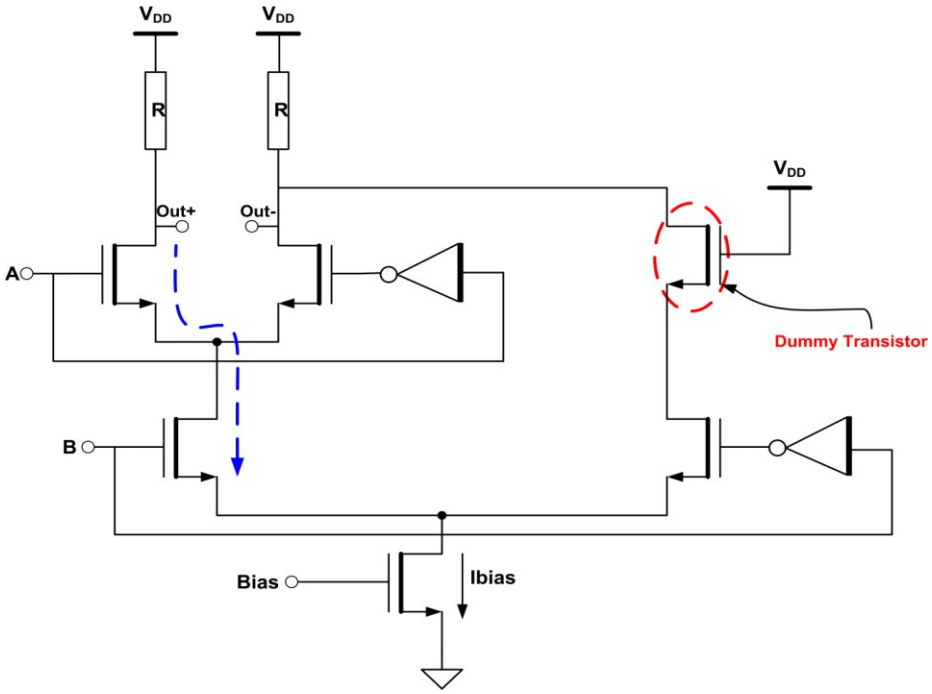

Fig. 6. MCML NAND/AND gate

Fig. 6. highlights MCML circuit used for the implementation of the encoder blocks. As the input pairs are fully differential the MCML topology offers good rejection to input supply noise change. The differential clocking mechanism also helps to maintain good linearity at very high frequencies [15]. All the blocks of the encoder have been realised using the MCML NAND/AND gate. This simplifies the circuit implementation and also allows for accurate monitoring of signal feed-through and feedback to and from the comparator array [16]. The common gate architecture greatly reduces the propagation delay time and also reduces problems during calculation of static power consumption [17], [18]. The advantage of the differential gate architecture is that the outputs can be treated as NAND or AND functionality.

4 Results

The high speed Flash Analog to Digital Converter was designed and simulated in Cadence Design Environment using standard V_T ST-Micro 90nm CMOS technology. The design was simulated based on a 1 V supply with a 1 V full-scale reference.
Fig. 7. to Fig. 9. show the linearity error variance and Spurious Free Dynamic Range (SFDR) for the 4 bit ADC. Fig. 10. Shows the different trip points for each of the comparators.

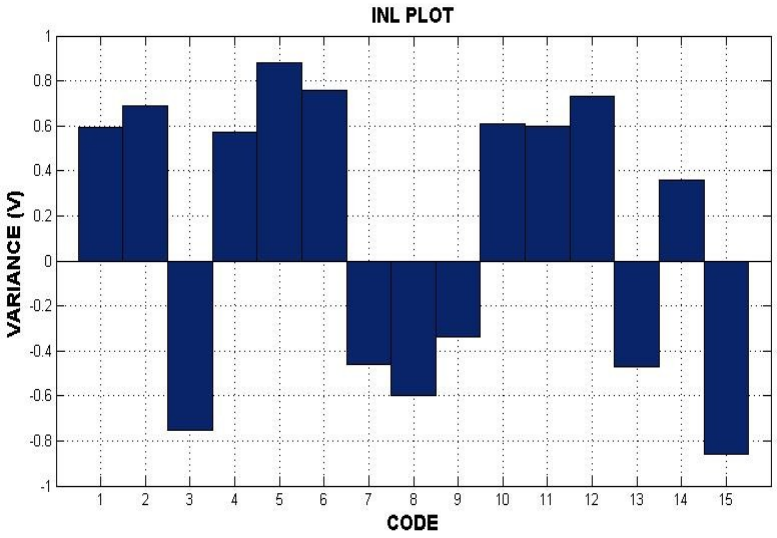

Fig. 7. Integral Non-Linearity Plot (f_{IN} = 800 MHz @ f_S = 4.1 Gsps)

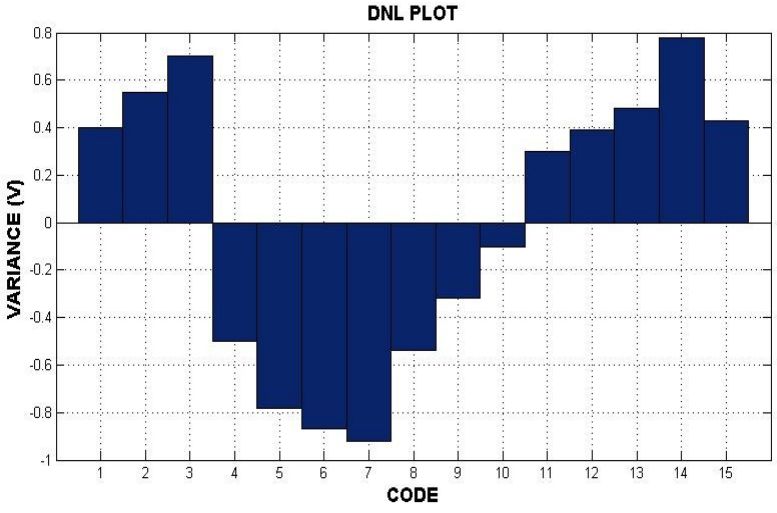

Fig. 8. Differential Non-Linearity Plot (f_{IN} = 800 MHz @ f_S = 4.1 Gsps)

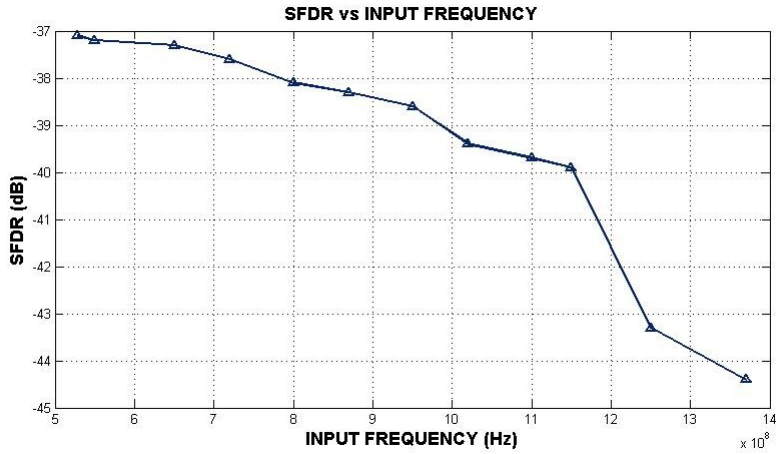

Fig. 9. Plot of SFDR versus Input Frequency

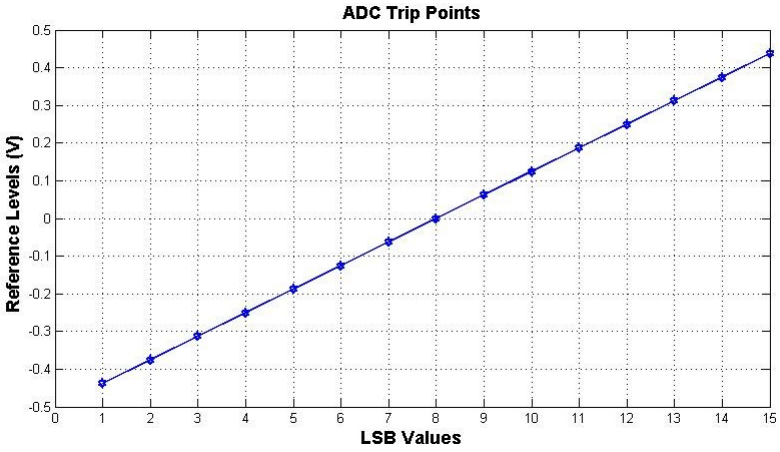

Fig. 10. Plot of ADC Trip Points

The performance characteristics of the ADC are detailed in Table 1. The entire ADC consumes 114 mW of power at input of 800 MHz sampled at 4.1 Gsps. The ADC has a linearity error variance of not more than ± 1 LSB. No Averaging or Interpolation techniques have been used to minimise the effects of offset. The encoder has been sized such that it has a maximum critical path delay of 0.234 ns. The encoder does not have any dynamic pipelining stages as there is no monotonicity error in the ADC, thereby reducing overall power dissipation.

Table 1. ADC Performance Characteristics

Parameter	**Performance Characteristic**		**[19]**	**[20]**
Input Signal Range	Sinusoidal 1 V p-p differential	Sinusoidal 1 V p-p differential	0.8 V p-p	1.6 V p-p
Input Frequency	800 MHz	1120 MHz	-	650 MHz
Resolution	4 bits (1LSB = 62.5 mV) differential	4 bits (1LSB = 62.5 mV) differential	4 bits	6 bits
Supply Voltage	1 V	1 V	1.8 V	3.3 V
Sampling Rate	4.1 Gsps	4.1 Gsps	3.2 Gsps	1.3 Gsps
Maximum Sampling Rate	6.3 Gsps	6.3 Gsps	3.2 Gsps	1.3 Gsps
Maximum INL	-0.82 V / +0.84 V	-0.96 V / +1.1 V	0.6 LSB	0.35 LSB
Maximum DNL	-0.92 V / +0.76 V	-1.4 V / +1.1 V	0.4 LSB	0.2 LSB
SFDR	-38.2 dB	-41.3 dB	-	> 44 dB
ENOB (@ 800 MHz)	3.45	3.1	3.6	> 5.5
Power	114 mW (@ 4.1 Gsps)	176 mW (@ 4.1 Gsps)	131 mW	500 mW
Structure	Non-Time Interleaved		2 Way Time Interleaved	Averaging
Technology	ST-Microelectronics 90 nm Standard V_T CMOS		0.18 um	0.35 um

5 Conclusion

This paper presents the design and of a high speed Flash Analog to Digital Converter for Ultra Wide Band Applications. The ADC achieves moderate linearity and resolution without the use of any power hungry offset averaging techniques. The Effective Number of Bits (ENOB) for a 800 MHz input is estimated as 3.45. The encoder was sized to provide high speed conversion with no pipelining. The ADC has very low gain low swing. No digital backend processing was required to correct ADC errors, such as mismatch and monotonicity.

Acknowledgments. The authors would like to thank Mr. David Fitrio for his technical expertise and critical insights.

References

1. Federal Communications Commission.: First Report and Order: Revision of Part 15 of the commissions rules regarding ultra wideband systems, ET Docket No. 98-153, FCC, 2002.
2. Australian Communications and Media Authority.: Use of ultra wideband approved for the first time, Media Release, Media Release No. 24, April 2004.
3. Oppermann, I., Hamalainen, M., Iinatti, J.: UWB: Theory and Applications, WILEY International Publishers, 2004.
4. Newaskar, P., Blazquez, R., Chandrakasan, A.: A/D precision requirements for digital ultra-wideband radio receivers, J. of VLSI Signal Processing Systems for Signal, Image, and Video Technology, vol. 39, 2005, pp. 175-188.
5. Romdhane, M., Loumeau, P.: Analog to digital conversion specifications for ultra wide band reception, Proc. of the Fourth IEEE Intl. Sym. on Signal Processing and Information Technology, December 2004, pp. 157- 160.
6. Fischer, R., Kohno, R.: DS-UWB Physical Layer Proposal Submission to IEEE 802.15 Task Group 3a, September 2005.
7. Roberts, R.: XtremeSpectrum CFP Document, IEEE P802.15-03/153r8. July 2003.
8. Geelen, G.: A 6 b 1.1 GSample/s CMOS A/D converter, *ISSCC Dig. Tech. Papers*, 2001, pp. 128-129.
9. Walden, H. R.: Analog to Digital Converter Survey and Analysis, IEEE J. on Selected Areas in Comm., vol. 17, April 1999, pp. 539-550.
10. Yoo, J., Choi, K., Tangel A.: A 1-GSPS CMOS Flash A/D Converter for System-on-Chip Applications, IEEE Computer Society Workshop on VLSI, 2001, pp. 135139.
11. Stojcevski, A. Le, H. P., Singh, J., Zayegh, A.: Flash ADC Architecture, IEEE Electronic Letters, vol. 39, March 2003, pp. 501-502.
12. Mohan, A., Zayegh, A., Stojcevski, A., Veljanovski, R.: Comparator For High Speed Ultra Wideband A/D Converter, Proc. of the Intl. Conf. on Communication, Computer and Power, Feb. 2007.
13. Mohan, A., Zayegh, A., Stojcevski, A., Veljanovski, R.: High Speed Ultra Wide Band Comparator in Deep Sub-Micron CMOS, Intl. Sym. On Integrated Circuits, ISIC2007, In Print.
14. Heo, S., Krashinsky, R., Asanovi´c, K.: Activity-Sensitive Flip-Flop and Latch Selection for Reduced Energy, 19th Conference on Advanced Research in VLSI, March 2001
15. Razavi, B.: Principles of Data Conversion System Design, IEEE Press, 1995.
16. Ismail, A., Elmasry, M.: A low power design approach for mos current mode logic, Proc. of 2003 IEEE Intl. SOC Conference, Sep. 2003, pp. 143–146.
17. Khabiri, S., Shams, M.: Implementation of mcml universal logic gate for 10 ghz-range in 0.13 μm cmos technology, Proc. of IEEE Intl. Symp. on Circuits and Systems, vol. 2, May 2004, pp. 653–656.
18. Anis, M., Elmasry, M.: Self-timed mos current mode logic for digital applications, Proc. of IEEE Intl. Symp. on Circuits and Systems, vol. 5, May 2002, pp. 113–116.
19. Naraghi, S., Johns, D.: A 4-bit analog-to-digital converter for high-speed serial links, Micronet Annual Workshop, April 26-27,2004, Aylmer, Quebec, Canada, pp. 33-34.
20. Choi, M., Abidi, A.: 6-b 1.3-Gsample/s A/D Converter in 0.35 um CMOS, IEEE Jnl. of Solid State Circuits, Vol. 36, No. 12, Dec 2001, p.p. 1847-1858.