



VLSI-SoC: Design Trends

Andrea Calimera, Pierre-Emmanuel Gaillardon, Kunal Korgaonkar, Shahar Kvatinsky, Andre Reis

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Andrea Calimera · Pierre-Emmanuel Gaillardon ·
Kunal Korgaonkar · Shahar Kvatinsky ·
Ricardo Reis (Eds.)


VLSI-SoC: Design Trends


28th IFIP WG 10.5/IEEE International Conference
on Very Large Scale Integration, VLSI-SoC 2020
Salt Lake City, UT, USA, October 6–9, 2020
Revised and Extended Selected Papers

Editors

Andrea Calimera 
Politecnico di Torino
Turin, Italy

Kunal Korgaonkar 
Technion – Israel Institute of Technology
Haifa, Israel

Ricardo Reis 
Universidade Federal do Rio Grande do Sul
Porto Alegre, Brazil

Pierre-Emmanuel Gaillardon 
University of Utah
Salt Lake City, UT, USA

Shahar Kvatinsky 
Technion – Israel Institute of Technology
Haifa, Israel

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Preface

This book contains extended and revised versions of the highest quality papers presented during the 28th edition of the IFIP/IEEE WG 10.5 International Conference on Very Large Scale Integration (VLSI-SoC 2020), a global system-on-chip design and CAD conference. The 28th edition of the conference was held during October 6–9, 2020, virtually from Salt Lake City, USA. Previous conferences have taken place in Edinburgh, Scotland (1981); Trondheim, Norway (1983); Tokyo, Japan (1985); Vancouver, Canada (1987); Munich, Germany (1989); Edinburgh, Scotland (1991); Grenoble, France (1993); Chiba, Japan (1995); Gramado, Brazil (1997); Lisbon, Portugal (1999); Montpellier, France (2001); Darmstadt, Germany (2003); Perth, Australia (2005); Nice, France (2006); Atlanta, USA (2007); Rhodes Island, Greece (2008); Florianopolis, Brazil (2009); Madrid, Spain (2010); Kowloon, Hong Kong (2011), Santa Cruz, USA (2012), Istanbul, Turkey (2013), Playa del Carmen, Mexico (2014), Daejeon, South Korea (2015), Tallin, Estonia (2016), Abu Dhabi, United Arab Emirates (2017), Verona, Italy (2018), and Cuzco, Peru (2019).

The purpose of this conference, sponsored by the IFIP TC 10 Working Group 10.5, the IEEE Council on Electronic Design Automation (CEDA), and the IEEE Circuits and Systems Society, with the in-cooperation of ACM SIGDA, is to provide a forum for the presentation and discussion of the latest academic and industrial results and developments as well as the future trends in the field of system-on-chip (SoC) design, considering the challenges of nano-scale along with state-of-the-art and emerging manufacturing technologies. In particular, VLSI-SoC 2020 addressed cutting-edge research fields like low-power design of RF, analog and mixed-signal circuits, EDA tools for the synthesis and verification of heterogenous SoCs, accelerators for cryptography and deep learning and on-chip interconnection systems, reliability and testing, and integration of 3D-ICs. The chapters of this new book in the VLSI-SoC series continue its tradition of providing an internationally acknowledged platform for scientific contributions and industrial progress in this field.

For VLSI-SoC 2020, 38 papers out of 74 submissions were selected for oral presentation, and out of those 38 full papers presented at the conference, 16 papers were chosen by a special selection committee to have an extended and revised version included in this book. The selection process for these papers considered the evaluation scores during the review process as well as the review forms provided by members of the Technical Program Committee and the session chairs as a result of the presentations.

The chapters of this book have authors from Belgium, Brazil, England, France, Germany, Israel, Italy, Japan, and USA. The Technical Program Committee for the regular tracks comprised 93 members from 23 countries.

VLSI-SoC 2020 was the culmination of the work of many dedicated volunteers: paper authors, reviewers, session chairs, invited speakers, and various committee chairs. We thank them all for their contributions.

This book is intended for the VLSI community at large, and in particular the many colleagues who did not have the chance to attend the conference. We hope that you enjoy reading this book and find it useful in your professional life and for the development of the VLSI community as a whole.

May 2021

Andrea Calimera
Pierre-Emmanuel Gaillardon
Kunal Korgaonkar
Shahar Kvatinsky
Ricardo Reis

Organization

The IFIP/IEEE International Conference on Very Large Scale Integration System-on-Chip (VLSI-SoC) 2020 took place during October 6–9, 2020, virtually from Salt Lake City, USA. VLSI-SoC 2020 was the 28th in a series of international conferences, sponsored by IFIP TC 10 Working Group 10.5 (VLSI), IEEE CEDA, and ACM SIGDA. The Organization Committee of the conference consisted of the following colleagues:

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Piero Malcovati	University of Pavia, Italy
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Yuanqing Cheng	Beihang University, China
Zhaohao Wang	Beihang University, China

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List of Contributors

Amin Aghighi Electrical and Computer Engineering Department, University of Utah, Salt Lake City, USA

Tutu Ajayi University of Michigan, Ann Arbor, MI, USA

Muhannad S. Bakir Georgia Institute of Technology, Atlanta, GA, USA

Rotem Ben-Hur Technion - Israel Institute of Technology, Haifa, Israel

Davide Bertozzi Department of Engineering, Università degli Studi di Ferrara, Ferrara, Italy

David Blaauw University of Michigan, Ann Arbor, MI, USA

Juergen Boemmels IMEC, Leuven, Belgium

Moreno Bragaglio Department of Computer Science, University of Verona, Verona, Italy

Benton Calhoun University of Virginia, Charlottesville, VA, USA

Francky Catthoor IMEC, Leuven, Belgium; KU Leuven, Leuven, Belgium

Chien-Hen Chen University of Virginia, Charlottesville, VA, USA

Yaswanth K. Cherivirala University of Michigan, Ann Arbor, MI, USA

Josie Esteban Rodriguez Condia Dip. di Automatica e Informatica (DAUIN), Politecnico di Torino, Torino, Italy

Wim Cops MACOM Technology Solutions, Sophia Antipolis, France

David Cordova MACOM Technology Solutions, Sophia Antipolis, France

Brian Crafton Georgia Institute of Technology, Atlanta, GA, USA

Shanshan Dai Brown University, Providence, RI, USA

Marina Deng University of Bordeaux, CNRS UMR 5218, Bordeaux INP Talence, Bordeaux, France

Yann Deval Laboratoire IMS, Université de Bordeaux, Bordeaux INP, CNRS UMR 5218, Talence, France

Ronald Dreslinski Jr. University of Michigan, Ann Arbor, MI, USA

Wenbo Duan University of Michigan, Ann Arbor, MI, USA

Adi Eliahu Technion - Israel Institute of Technology, Haifa, Israel

Behrouz Farhang-Boroujeny Electrical and Computer Engineering Department, University of Utah, Salt Lake City, USA

Morteza Fayazi University of Michigan, Ann Arbor, MI, USA

Masahiro Fujita The University of Tokyo, Tokyo, Japan

Pierre-Emmanuel Gaillardon University of Utah, Salt Lake City, UT, USA

Jonas Gava Instituto de Informática, PGMicro, Universidade Federal do Rio Grande do Sul - UFRGS, 9500, Porto Alegre, Brazil

Samuele Germiniani Department of Computer Science, University of Verona, Verona, Italy

Edouard Giacomini University of Utah, Salt Lake City, UT, USA

Shourya Gupta University of Virginia, Charlottesville, VA, USA

Kangping Hu Brown University, Providence, RI, USA

Yinghua Hu University of Southern California, Los Angeles, CA, USA

Sumanth Kamineni University of Virginia, Charlottesville, VA, USA

Ankit Kaul Georgia Institute of Technology, Atlanta, GA, USA

Sumanth Kolluru University of Utah, Salt Lake City, USA

Tushar Krishna Georgia Institute of Technology, Atlanta, GA, USA

Milos Krstic IHP - Leibniz-Institut für innovative Mikroelektronik, Frankfurt Oder, Germany

Abhishek Kumar Université de Toulouse, LAAS, CNRS, INP Toulouse, Toulouse, France

Shahar Kvatinsky Technion - Israel Institute of Technology, Haifa, Israel

Kyumin Kwon University of Michigan, Ann Arbor, MI, USA

Herve Lapuyade Laboratoire IMS, Université de Bordeaux, Bordeaux INP, CNRS UMR 5218, Talence, France

Guilhem Larrieu Université de Toulouse, LAAS, CNRS, INP Toulouse, Toulouse, France; Institute of Industrial Science, LIMMS-CNRS/IIS, The University of Tokyo, Tokyo, Japan

Sebastien Le Beux Lyon Institute of Nanotechnology, University of Lyon, CNRS UMR 5270, Lyon, France; Ecole Centrale de Lyon, Ecully, France

Aurélien Lecestre Université de Toulouse, LAAS, CNRS, INP Toulouse, Toulouse, France

Jeongsup Lee University of Michigan, Ann Arbor, MI, USA

Xiaoyu Lian Brown University, Providence, RI, USA

Sung-Kyu Lim Georgia Institute of Technology, Atlanta, GA, USA

Cristell Maneux University of Bordeaux, CNRS UMR 5218, Bordeaux INP Talence, Bordeaux, France

François Marc University of Bordeaux, CNRS UMR 5218, Bordeaux INP Talence, Bordeaux, France

Cedric Marchand Lyon Institute of Nanotechnology, University of Lyon, CNRS UMR 5270, Ecole Centrale de Lyon, Ecully, France

Alan Mishchenko UC Berkeley, Berkeley, CA, USA

Yukio Miyasaka UC Berkeley, Berkeley, CA, USA

Chhandak Mukherjee University of Bordeaux, CNRS UMR 5218, Bordeaux INP Talence, Bordeaux, France

Gauthaman Murali Georgia Institute of Technology, Atlanta, GA, USA

Shahin Nazarian University of Southern California, Los Angeles, CA, USA

Nicolas Nodenot MACOM Technology Solutions, Sophia Antipolis, France

Pierluigi Nuzzo University of Southern California, Los Angeles, CA, USA

Ian O'Connor Lyon Institute of Nanotechnology, University of Lyon, CNRS UMR 5270, Ecole Centrale de Lyon, Ecully, France

Luciano Ost Wolfson School, Loughborough University, Loughborough, England

Yohan Piccin MACOM Technology Solutions, Sophia Antipolis, France

Arnaud Poittevin Lyon Institute of Nanotechnology, University of Lyon, CNRS UMR 5270, Ecole Centrale de Lyon, Ecully, France

Graziano Pravadelli Department of Computer Science, University of Verona, Verona, Italy

Arijit Raychowdhury Georgia Institute of Technology, Atlanta, GA, USA

Sherief Reda Brown University, Providence, RI, USA

Ricardo Reis Instituto de Informática, PGMicro, Universidade Federal do Rio Grande do Sul - UFRGS, 9500, Porto Alegre, Brazil

François Rivet Laboratoire IMS, Université de Bordeaux, Bordeaux INP, CNRS UMR 5218, Talence, France

Ronny Ronen Technion - Israel Institute of Technology, Haifa, Israel

Jacob K. Rosenstein Brown University, Providence, RI, USA

Julien Ryckaert IMEC, Leuven, Belgium

Mehdi Saligane University of Michigan, Ann Arbor, MI, USA

Rakshith Saligram Georgia Institute of Technology, Atlanta, GA, USA

Tannu Sharma University of Utah, Salt Lake City, USA

Matteo Sonza Reorda Dip. di Automatica e Informatica (DAUIN), Politecnico di Torino, Torino, Italy

Samuel Spetalnick Georgia Institute of Technology, Atlanta, GA, USA

Kenneth S. Stevens University of Utah, Salt Lake City, USA

Dennis Sylvester University of Michigan, Ann Arbor, MI, USA

Armin Tajalli Electrical and Computer Engineering Department, University of Utah, Salt Lake City, USA

Caleb R. Tulloss Columbia University, New York, NY, USA

Alessandro Veronesi IHP - Leibniz-Institut für innovative Mikroelektronik, Frankfurt Oder, Germany

John Wawrzynek UC Berkeley, Berkeley, CA, USA

David D. Wentzloff University of Michigan, Ann Arbor, MI, USA

Kaixin Yang University of Southern California, Los Angeles, CA, USA