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Abstract. Challenges were introduced in integrated circuits design due to the technology scaling. The evolution of integrated circuits has made them more susceptible to the radiation effects, besides increasing the manufacturing process variability. These challenges can lead to circuits operating outside their specification ranges. Transistor arrangement influences the performance of logic cells; complex logic gates can be used to minimize area, delay and power consumption. However, with the increasing relevance of nanometer challenges, it is necessary also to consider these factors at logic level design. This work explores different transistor arrangements for a set of logic functions at the layout level to evaluate the SET response under the process variability. The process variability is analyzed through the work-function fluctuations of the metal gate. The complex gate and the multi-level of NAND2 topologies, that implement the same function, were designed using the 7nm FinFET ASAP7 Process Design Kit. Results show that the multi-level topology is more robust to the radiation effects at both ideal fabrication process and considering the process variability impact. The LETth value considering the multi-level topology is on average 55% higher than the values considering the complex topology. Moreover, all the logic functions analyzed independently of the topology are more sensitive to the SETs considering the impact of the process variability.

Keywords: FinFET technology · Multi-level design · Process variability · Soft errors · Single event transient

1 Introduction

The radiation-induced soft errors and the process variability are an essential reliability concern for nanotechnologies, affecting integrated circuits used for

space or even terrestrial applications [1, 2]. Variability is related to the random deviation, which causes an increase or decrease of typical design specifications. The primary variability issue is the uncertainty about the correct operation of the circuit. There is no guarantee that a circuit will behave as expected after the manufacturing process. Due to the variability effects, each circuit can present a different electrical behavior such as abnormal power consumption, performance deviation, or both. The unexpected behavior due to variations can stimulate circuit degradation besides make it inappropriate for your initial purpose.

Electronic circuits operating in space, especially in harsh environments, may be exposed to significant radiation doses as well as to the incidence of heavy particles from the sun or from outside the galaxy. From this exposure to radiation, changes and disturbances in the circuit can occur with high probability. Degradations that arise due to the incidence of a single particle are called Single Event Effects (SEE). If this single-particle causes a permanent failure in the circuit, it is considered a hard error. In case of an error in the system that does not cause permanent damage, it is called Single Event Transient (SET) or Non-Destructive (soft error) [3, 4].

For a long time, SETs were not considered a significant reliability concern. The logical, electrical and latching window masking present in digital logic, were enough to minimize the importance of considering the phenomenon. However, with technology scaling, lower supply voltages and reduced nodal capacitances, the minimum charge required to induce a transient pulse was decreased [2, 5]. Also, it is more likely that a SET generated in combinational logic will be captured at the storage element due to the higher operating frequencies. Thus, to overcome some of these problems, new device architectures and novel materials are being used.

Multigate devices have allowed the further scaling of transistors by providing better control of Short-Channel Effects (SCE), lower leakage currents and better yield [6]. On multigate devices, variability effects are mainly due to the work-function fluctuation (WFF) of the metal gate [7, 8]. FinFET (Fin-Shaped Field Effect Transistor) technology is the main multigate device replacing bulk MOSFET devices in sub-22nm technology nodes [7]. Due to its limited sensitivity volume compared to planar devices, the charge collection region is reduced in this technology [9, 10], showing a better response to radiation effects, even considering the technology scaling. However, the radiation effects are not negligible on multigate devices [11].

The proper estimation of Threshold Linear Energy Transfer (LETth) along with the SET pulse width is of utmost importance for soft error (SE) mitigation and radiation-tolerant circuit design [12]. Also, few papers analyze the impact of process variability on the SET. The impact of process variability on on-state (I_{on}) and off-state (I_{off}) currents using FinFET technology in a set of technological nodes ranging from 20nm to 7nm is compared in [13]. The prominence is in the evaluation of Metal Gate Granularity (MGG) impact on the work-function (WF) of the gate. The results demonstrate the importance of not only evaluating

variations in threshold voltage but also in other parameters and the significant influence of WFF in the threshold voltage and the I_{on} and I_{off} currents.

Regarding the radiation effects, a comparative soft error evaluation of logic gates in bulk FinFET technology using various technological nodes is presented in [9]. The main objective is allowing for estimating the SER of logic gates for ground applications, as well as for understanding the impact of voltage and drive strength through analysis o the sensitivity to soft errors. Also, similar work highlights the robustness of the 7nm FinFET technology, considering other logic functions [14] and also majority voter circuits [15]. The latter also analyzes the impact of process variability on the SET.

In this context, this work investigates the radiation robustness, considering the process variability effects, of a set of logic functions implemented in two different transistor topologies using 7nm FinFET technology [16]. The SET pulse width was obtained and the LETth was calculated to characterize the SET response. First, a radiation robustness analysis is performed considering only the ideal behavior, and then the process variability impact is considered. The main contributions of this work are: 1) to provide an evaluation of the SET sensitivity trends for complex logic gates, exploring the use of different transistor arrangements; 2) to consider the impact of process variability effects and radiation sensibility together on the analysis, and 3) to present a detailed investigation about the topology relation with the FinFET logic cells robustness through the LETth.

Next Section summarizes the main radiation effects, including their origins and the behavior on FinFET devices. Section 3 presents the process variability effects on FinFET technology, focusing on the WFF of the metal gate. Section 4 describes the methodology steps to observe these effects on multi-level and complex gate designs. With the set of information from the evaluations, this work discusses the results in Section 5 and present the main conclusions in Section 6.

2 Radiation Effects

The dynamic scaling alongside the low supply voltages, large transistor density, and the high-frequency operation introduce new reliability issues in integrated circuits, such as the high Single Event Effects (SEE) sensitivity and multi-charge collection [9, 17]. This chapter presents the main concepts and characteristics of the radiation effects on electronic circuits. The focus is on SEEs, especially the impact of transient faults on devices. Before detailing these effects, it is important to present their origins.

Anomalies induced by the radiation effects on electronic circuits are known from the beginning of space exploration. The research aimed at the study of the radiation effects on electronic circuits was initially considered a concern of utmost relevance only in projects developed for military or space applications. The Earth is protected by the atmosphere, which acts as a semi-permeable “screen”, to let throughout light and heat, while stopping radiation and ultraviolet rays (UVs) [3]. The intensity of the radiation basically increases according to the increase

in altitude relative to ground level. However, due to phenomena related to the earth's magnetic field (the polar regions are an example), some regions suffer from a higher intensity of radiation even though they are located at low altitudes.

In space and the Earth's atmosphere, there is a diverse range of radiation, which is classified into two broad groups: ionizing particles and non-ionizing particles. The main particles that may cause unwanted effects in electronic circuits are electrons, protons, neutrons, muons, alpha particles and heavy ions, as well as electromagnetic radiation, such as x-rays and gamma rays [4]. At sea level, muons are the most numerous terrestrial species [18]. The primary components of radioactive phenomena encountered in space can be classified into four categories by origin: Radiation belts, solar flares, solar wind and cosmic rays [3]. Fig. 1 shows the relationship between the Sun and the Earth that gave rise to these phenomena.

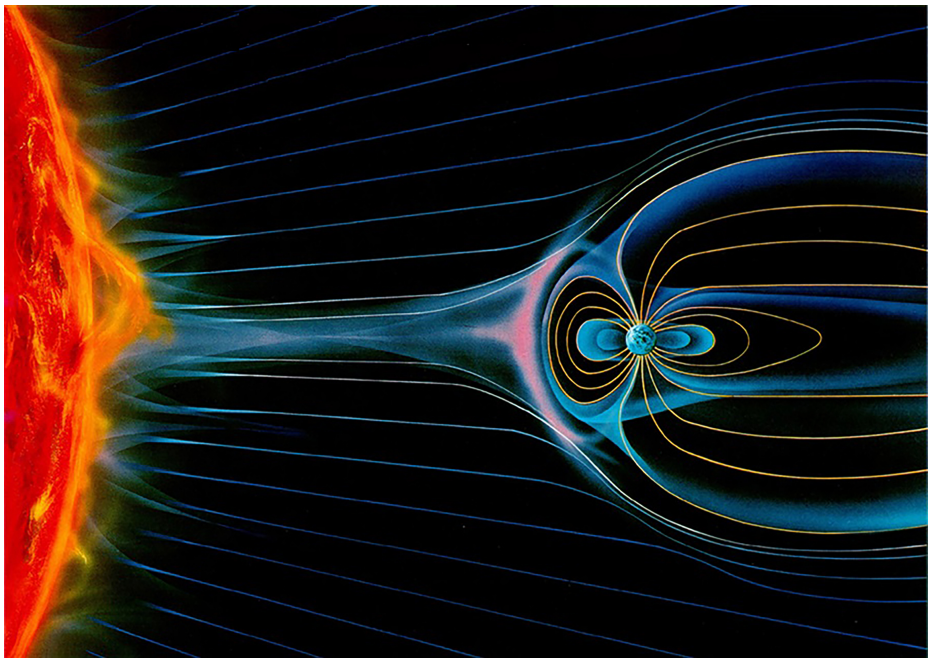


Fig. 1. Radiation effects from the Sun-Earth relationship [19].

2.1 Characterization of the Radiation Effects on Electronic Devices

The effects related to the incidence of radiation in electronic components have been studied for a long time by the international scientific community, mainly for space and military applications. The integrated circuits that experience the interaction of ionizing particles basically suffer from two types of degradation:

those of singular character, occurring due to the incidence of a single particle, and those of a cumulative nature, which occur due to the accumulation of doses of ionizing radiation over the lifetime of the circuit.

Cumulative effects have their origin due to the dose of ionizing radiation accumulated over the life of the device and are classified as Total Ionizing Dose (TID). Prolonged exposure to ionizing radiation, due to accumulated (radiation-induced) electric charges, causes parts of the circuit to change in their electrical characteristics, such as a change in threshold voltage (V_{th}) and the increase in the leakage current of the device. These electrical changes impair the correct functioning of the device and may, depending on the amount of accumulated dose, permanently damage it.

The TID response of bulk silicon and SOI FinFETs are significantly different in terms of radiation-induced V_{th} and I_{off} current. Bulk silicon FinFET radiation tolerance is reduced due to an increase in I_{off}, and SOI FinFET radiation tolerance is reduced due to V_{th} shifts [20]. Bulk FinFETs have a similar TID response as planar bulk MOSFETs, that is, the buildup of oxide-trapped charge in the STI triggers a parasitic lateral transistor that modifies the electrical characteristics (higher I_{off}) [21]. Degradations that occur due to the incidence of a single particle are called Single Event Effects (SEE), these effects will be presented with more details next.

Single Event Effects The Single Event Effects occur due to the interaction of large ionizing particles (protons, neutrons, α particles and heavy ions) that pass through insulation, semiconductor layers, or even all MOS device. These particles, when entering the silicon material, generate a transient path composed of ionized elements (electron-hole pairs - e^-/h) arranged under a radial distribution that permeates the path of the incident particle. This transient path may have sufficient mobile charge to drive a current pulse against the presence of the external electric field due to the polarization of the transistor [22].

SEEs indicate any measurable or observable change in a state or performance of a nanoelectronic device, component, subsystem or system (digital or analog) as a result of the incidence of a single energetic particle. According to the intensity and the region in which this current flows, it is capable of causing faults that may be permanent in the device structure, called destructive events (hard error), or non-destructive (soft errors), represented by the Single Event Transient (SET) and the Single Event Upset (SEU) [23]. Fig. 2 presents the classification of the major SEEs in the literature. The focus of this work is the SET effect, which occurs in combinational circuits.

The most common transient effects on combinational circuits are the SETs, in which the incidence of an ionized particle produces a transient pulse that can propagate through a logic path and be latched by memory elements. The transient pulse is generated by the interaction of energetic particles near a sensitive region of a transistor when the collected charge (Q_{coll}) exceeds the critical charge (Q_{crit}). However, in sub-22nm technological nodes other phenomena must also be considered in the characterization of the transient pulse. The influence of charge-

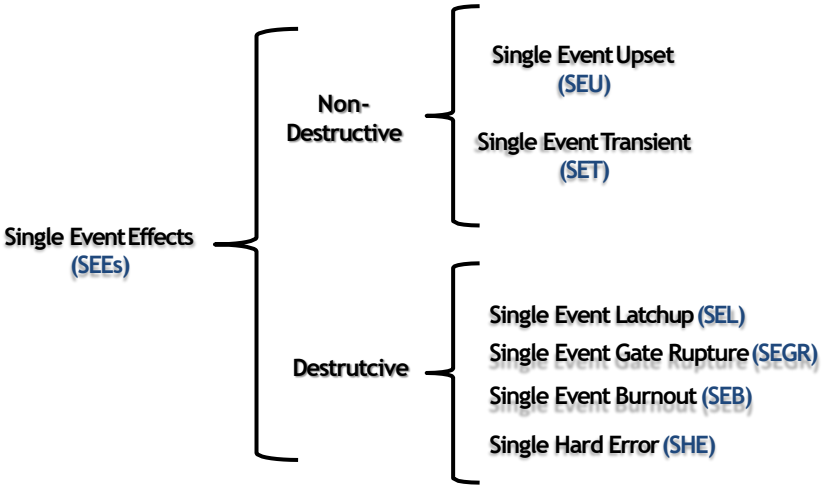


Fig. 2. Classification of major Single Event Effects. Modified from [24].

sharing (charge collected by multiple transistors for a single incident particle) mechanism does not seem to have diminished for the FinFET technology. TCAD results show the extent of electrical perturbations and charge-sharing similar to what has been observed for older technologies. This effect can cause the pulse quenching in ion-induced transients, resulting in a reduced overall sensitivity of the system against SEE [25].

To quantify the SET effects, characteristics such as amplitude, shape and current pulse duration are important quantities [26]. The amplitude and duration of a SET depend on factors such as the fabrication technology, the circuit geometry, the bias voltage of the affected node, node load impedance, location of the transistor reached by the particle, in addition to factors related to the SEE itself, as the type and energy of the incident particle [26].

The energy deposited by a particle due to its ionization in silicon is an essential metric in the study of radiation effects in nanotechnologies because it is directly related to the magnitude of the generated transient pulse. Linear Energy Transfer (LET) (shown in Eq. 1) is the amount of energy that a particle releases per unit of compliance from the path traveled by it.

$$LET = \frac{\partial E}{\partial x} \tag{1}$$

The LET is dependent on the mass and energy of the particle and the ionized material, so particles with higher mass and energy ionized in denser materials have higher LETs [27]. Threshold LET (LETth) is the minimum LET to cause an effect in the circuit [11].

The disruptive nature of the FinFET structure introduces questions in terms of understanding, predicting and mitigating SEEs in circuits. The 3D structure of FinFET devices is favorable to reduce the soft error vulnerability according to several works available in the literature [10, 28, 29]. This reduction of the soft error vulnerability happens because the sensitive areas of FinFETs are little exposed to the charge collection region as shown in Fig 3. FinFET technologies collect significantly less charge than conventional planar technologies. The work of [30] indicates that charge collection for semiconductor regions in FinFET technologies is approximately reduced by 70% compared to planar technologies. From a design standpoint, the accurate estimation of SEE susceptibility is crucial to ensure reliable circuits.

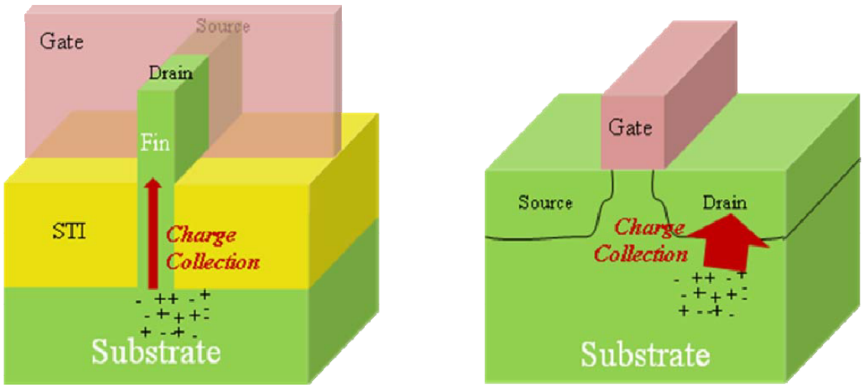


Fig. 3. Comparison of charge collection mechanism between FinFET devices and Planar CMOS technologies [29].

Although FinFET technology is more robust to soft errors than planar technologies, there are still many concerns that justify the study of this device. The process variability, one of the main challenges in sub-22nm technologies, can modify the LETth to induce a soft error. Ultra-Low-Power (ULP) circuits are increasingly being used, and low voltages increase the probability of SE occurrence. Also, with the demand for devices increasingly faster, the operation frequency increases, also increasing the possibility of a memory element capturing a SE.

3 Process Variability Effects on FinFET Devices

The variability in electronic circuits can be divided into three different factors: environmental, reliability and physical [31]. Environmental factors appear during the circuit operation; variations in supply voltage and temperature are examples

of environmental factors. Reliability factors are related to the transistor aging, due to the high electric fields presented in modern circuits. Finally, physical factors are associated with variations in electrical and geometrical parameters, which may occur due to the manufacturing process of the devices [31]. The latter is best known for process variability and is the focus of this study. This chapter details the main features of the process variability, showing its impact on FinFET devices and highlighting the most significant parameter for their effects.

The primary sources of process variability at nanometer nodes are due to the sub-wavelength lithography [31, 32]. The variability on geometric parameters impact directly the transistor threshold voltage. These variations can compromise the entire blocks of cells or reduce the performance and energy efficiency of the chip. Some expected sources of variability for FinFETs are highlighted in [33]: the influence of variations in the fins height, the width variations across the double-standard layers, the variations of the fin to fin, the dependent variations the width of the pitch, the resistance of MOL (Middle of Line), and variations due to the overlap and the epitaxy. The main FinFET parameters and possible variability sources are shown in Fig. 4.

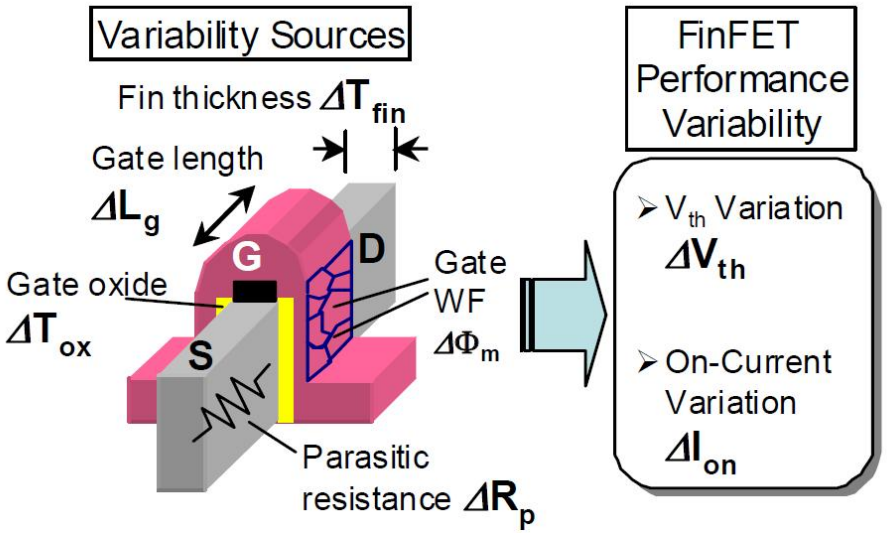


Fig. 4. Possible sources of FinFET variability [34].

For nanotechnology bulk CMOS devices, the geometric variability in the gate length has the greatest impact on the change of I_{on} current due to the random fluctuation in the dopants of the channel [35]. However, in FinFET devices, another parameter has a more significant impact. As a result of the active format of the fins, the fin channel is weakly doped to minimize variations in V_{th}. As

a consequence, the V_{th} of weakly doped channels is mainly configured by the working-function of the metals adopted in the gate. The use of metal as gate material introduced some fluctuation in the work-function of the gate, mainly due to the presence of MGG.

Thus, although variations in gate length, fin height and fin width influence the electric behavior of FinFET devices, the fluctuations of the metal gate work-function are the main source of expected variability for FinFETs sub 20nm [36, 37, 13]. Fig. 5 illustrates this behavior considering the impact on the I_{on} current.

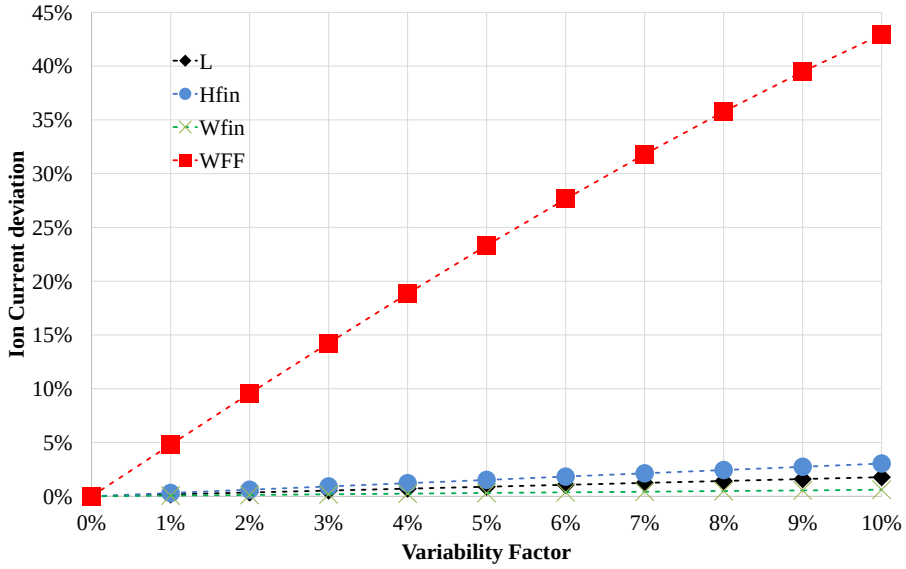


Fig. 5. Impact on I_{on} current due to work-function fluctuation [13].

In the ideal fabrication process, metal gates devices have the gates produced with a unique metal uniformly aligned and very lower work-function deviation. Nevertheless, in a real fabrication process, metal gate devices are generally produced with metals with different WF randomly aligned that implies in higher WFF. WFFs are locally induced due to the polycrystalline nature of the metal lead to potential surface variations, and it is caused by the dependency of metal WF on the orientation of its grains, as illustrates the Fig. 6. The V_{th} fluctuation due to MGG is close to a Gaussian distribution, and the standard deviation is almost linearly proportional to metal-grain size [32].

4 Methodology

This work explores different transistor arrangements for a set of four logic functions (OAI21, OAI22, AOI211 and XOR) at the layout level to evaluate the SET

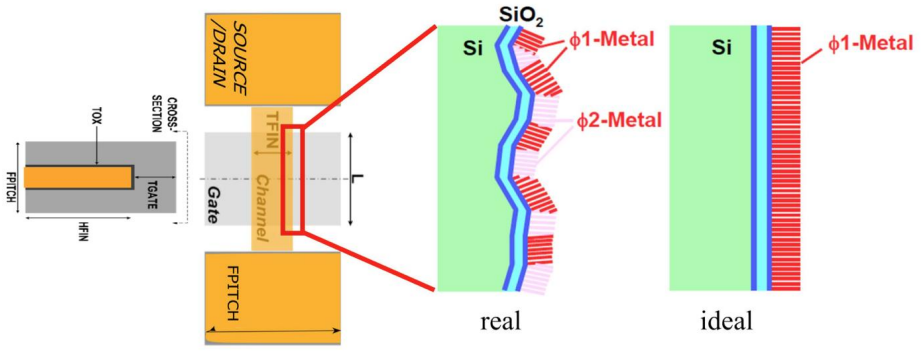


Fig. 6. FinFET devices: main geometric parameters and the random alignment of metal in real devices. Modified from [32] and [13].

response under the process variability. Two different topologies of transistor arrangement are investigated: 1) complex gate: optimized functions designed as a complex logic gate CMOS topology; and 2) the multi-level logic of NAND2 gates: the functions are converted using De Morgan's theorem into the only NAND2 transistor arrangements. Previous experiments also considered topologies using only NOR2 and a mix of NAND2-NOR2-INV. However, the only NAND2 topology proved to be better, and it was chosen for this study [38]. Table 1 and Table 2 present the logic functions and the equations for the complex gate version and the converted multi-level logic composed by NAND2 version, respectively. Although they represent the same functions, the versions are intrinsically different, which is interesting, since the comparison of similar versions does not present many advantages about the variability [39]. Fig. 7 presents the schematics of the OAI21 gate in its two versions highlighting all the sensitive nodes that were considered in the worst radiation sensitive case evaluation, which will be described in subsection 4.1.

Table 1. Complex gate functions. Modified from [40]

Logic Function	Complex Gate
OAI21	Y = (A+B . C)'
OAI22	Y = (A+B . C+D)'
AOI21	Y = (A.B + C + D)'
XOR	Y = A.B' + A'.B

All layouts were designed using the 7nm FinFET ASAP7 Process Design Kit (PDK), developed by Arizona State University in partnership with ARM [16]. Among the different models and corners available on this PDK, this work considers the regular threshold voltage (RVT) transistor model at typical (TT)

Table 2. Multi-Level Logic functions. Modified from [40]

Logic Function	Multi-level version with NAND2 gates
OAI21	Y = (((A.A)' . (B.B)')' . C)'
OAI22	Y = (((A.A)' . (B.B)')' . ((C.C)' . (D.D)')')'
AOI211	Y = (X . X)' | X = (((A.B)'.(((C.C)'.(D.D)')'.((C.C)'.(D.D)')')'
XOR	Y = ((A . (B.B)')' . ((A.A)' . B)')'

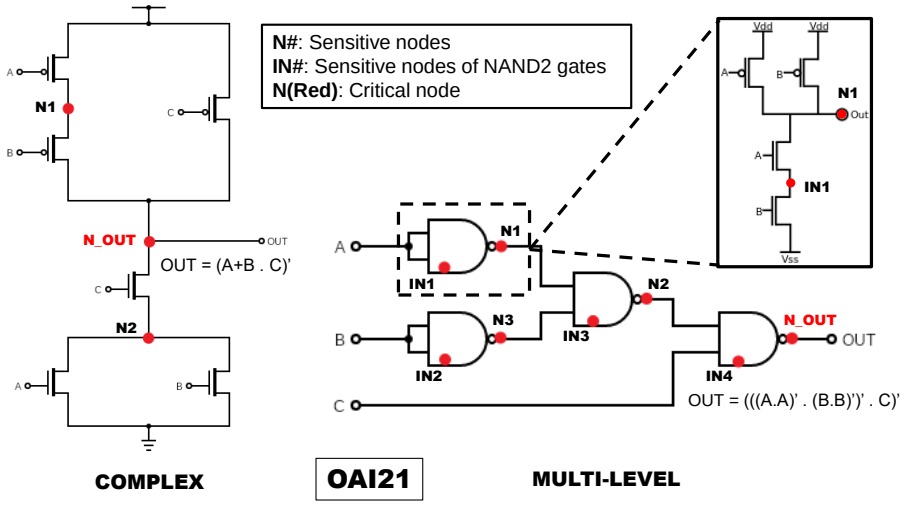


Fig. 7. OAI21 schematic in complex and multi-level transistor arrangements. Modified from [40].

corner. Table 3 summarizes the key devices parameters of 7nm FiFET ASAP technology. The nominal supply voltage is 0.7V, at a typical temperature of 25^{o}C.

The layout of all cells adopts three fins as transistor sizing as recommended in the PDK to allow the internal routing of the cells [16]. The cell height is set to 7.5 tracks of metal 2 (M2) that correspond to 0.27μm for all evaluated cells. The PDK assumes Extreme Ultraviolet (EUV) lithography for key layers, a decision based on its present near cost-effectiveness and resulting simpler layout rules. Non-EUV layers assume appropriate multiple patterning schemes, i.e., self-aligned quadruple patterning (SAQP), self-aligned double patterning (SADP) or litho-etch litho-etch (LELE), based on 193nm optical immersion lithography [16]. The design rules, actual dimensions and underlying assumptions for some major layers are shown in Table 4.

The specific design rule derivation is explained for key layers at the front end of line (FEOL), middle of line (MOL) and back end of line (BEOL) of the predictive process modeled. As an example, the layout of OAI21 gate is

Table 3. Key parameters of 7nm FinFET ASAP technology [16]

Parameters		7nm
Supply Voltage		0.7V
Gate Length (L_G)		21nm
Fin Width (W_{FIN})		6.5nm
Fin Height (H_{FIN})		32nm
Oxide thickness (Tox)		2.1nm
Channel Doping		$1\times10^{22}m^{-3}$
Source/Drain Doping		$2\times10^{26}m^{-3}$
Work Function	**NFET**	4.3720eV
	PFET	4.8108eV

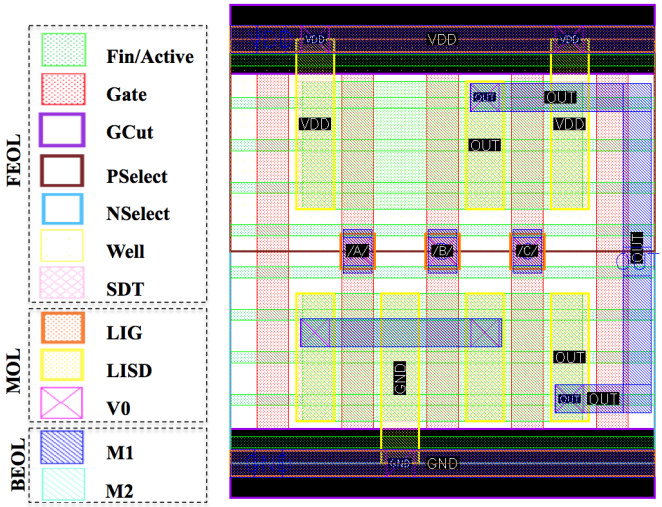
presented on Fig. 8a and Fig. 8b in complex gate and multi-level logic topologies, respectively.

All layouts were validated by Design Rule Check (DRC) and Layout Versus Schematic (LVS) steps. The extracted netlist with parasite capacitances is obtained and it was used for the radiation sensitivity evaluation. From the extracted netlist, SPICE simulations are performed. The input switching frequency is set at 500MHz and inverters are connected to the input sources introducing realistic delays to the cells. The project flow carried out in this work can be seen in Fig. 9.

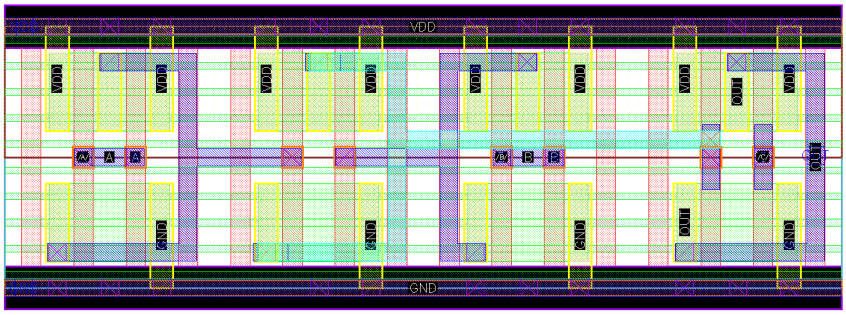
Table 4. Key layer lithography assumptions, widths and pitches [16]

Layer	Lithography	Width/drawn (nm)	Pitch (nm)
Fin	SAQP	6.5/7	27
Active (horizontal)	EUV	54/16	108
Gate	SADP	21/20	54
SDT/LISD	EUV	25/24	54[b]
LIG	EUV	16/16	54
VIA0–VIA3	EUV	18/18	25[a]
M1–M3	EUV	18/18	36
M4 and M5	SADP	24/24	48
VIA4 and VIA5	LELE	24/24	34[a]
M6 and M7	SADP	32/32	64
VIA6 and VIA7	LELE	32/32	45[a]
M8 and M9	SE	40/40	80
VIA8	SE	40/40	57[a]

[a] Corner to corner spacing as drawn.
[b] Horizontal only.



(a) OAI21



(b) OAI21_NAND

Fig. 8. OAI21 layout in the two topologies: (a) complex and (b) multi-level of NAND2 [40].

The SET fault injection is modeled as the Messenger's equation shown in Eq. 2 [41], where *Qcoll* is the collected charge, τ_α ($1.64 \times 10^{-10} s$) is the collect charge timing constant, τ_β ($5 \times 10^{-11} s$) is the timing constant to establish the ion track and L ($21nm$) is the charge collection depth. The values used in this work are the typical values used for simulations and experiments in silicon presented in [42], but modified to better characterize recent technologies, such as FinFET. This effect is reproduced on the SPICE simulation as a current source, simulating the SET effects on the transistors.

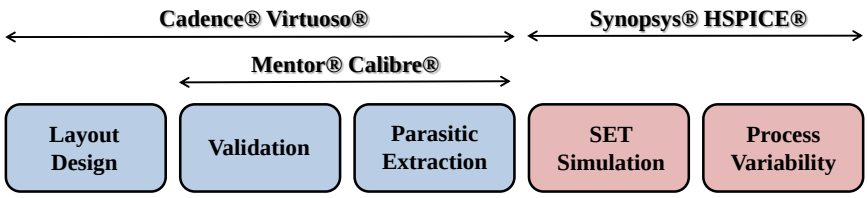


Fig. 9. Project flow for all analyzes [40].

$$I(t) = \frac{Qcoll}{\tau_\alpha - \tau_\beta}(e^{-\frac{t}{\tau_\alpha}} - e^{-\frac{t}{\tau_\beta}})$$
$$Qcoll = 10.8 \times L \times LET \tag{2}$$

4.1 Worst Radiation Sensitive Case

The first step in the radiation sensitivity evaluation was to identify the most sensitive node and input vector at each circuit. A fault injection campaign for a particle with LET estimated to 58 Mev.cm^2/mg was performed at each node of the circuits, as shown in Fig. 7 considering all possible input vectors. The definition of 58 Mev.cm^2/mg as the LET value used for the fault injection campaign was performed considering the highest LET that still characterizes a simulation at the ground level (LET $\leq$ 60 Mev.cm^2/mg) [43, 44]. Two inverters were used for each input of the circuit and a single inverter for the output, to emulate the worst fan-out scenario, i.e. lowest fan-out (FO1). Consider the amplitude and the width of the SET pulses allow determining which node and input vector are the most sensitive [11] and characterize the worst radiation sensitive case. After the worst radiation sensitive case was obtained, each logic gate was fault injected considering this sensitive scenario, i.e., the most critical node, the sensitive input vector and the waveform of the pulse (strikes at P-type devices or N-type devices).

4.2 The SET response at the Ideal Fabrication Process

This step evaluates the circuit under radiation effects but the effects of process variability are not considered. The LETth and the SET pulse width are used to characterize the SET response. Before starting the fault injection in the circuit, it is important to know the worst-case delay of each logic gate, which will be used to determine the LETth. Thus, the worst-case delay of each logic function considering both topologies was obtained. In this work, it is considered the SET effects, more specifically, when a transient pulse propagates to the inverter

chain output. To calculate the LETth, two characteristics of the SET pulse were considered: amplitude and width. A fault in the circuit is considered when the SET pulse amplitude exceeds half of the nominal supply voltage ($V_{DD}/2$) and the SET pulse width is greater than the circuit worst-case delay. That is, the metrics of the worst-case delay and the SET pulse width are used in obtaining the LETth, which is the primary metric used in this work. These values are used as a form of reference values to evaluate the process variability effects.

4.3 Process Variability Analysis

The analysis considering the process variability effects is performed keeping the same configurations of the previous step, however, considering the impact of the process variability through the WFF. Metal gate devices suffer from the WFF caused by the misalignment of metal grains in the gate. This fluctuation exhibits a multi-nominal distribution, which can be approximated by a Gaussian distribution if the number of grains on the surface of metal-gate is high enough (>10) [45], which corresponds to the FinFET ASAP7 model characteristics. The WFF effect due to process variation is explored through the statistical Monte Carlo simulation process, considering a Gaussian distribution with a 3-sigma deviation of 5% the WFF [13]. Two thousand simulations were run for each logic gate [45]. No correlation between different types of transistors was assumed, which means that PFET and NFET devices may come up with different variations in its parameters. Timing, SET pulse amplitude and width measurements were taken for each Monte Carlo simulation. The mean (μ) of these values is considered to calculate a new LETth, i.e., a LETth that considers the process variability impact. Also, the standard deviation (σ) of the mean values is obtained and a robustness analysis is performed using the normalized standard deviation (σ/μ) of the SET pulse width. The σ/μ is used to define how much a circuit is sensitive to process variability. The lower are the values of this ratio; the more robust to variability are the circuits.

5 Results

The worst radiation sensitive case was obtained before characterizing the SET response. The critical node, the most sensitive input vector and the transient pulse format, which compose the worst-case scenario for each logic function in both topologies are presented in Table 5.

To characterize the fault at a given node of the circuit, it is evaluated whether the SET pulse propagates to the circuit output. Thus, the probability of the critical node being the output itself is very high and this behavior is proven in the obtained results for both topologies. It can be seen that the most sensitive input vectors vary even considering the same logic function, due to the use of a different transistor arrangement. For OAI21 and AOI211 gates this difference between the input vectors is reflected in the format of the transient pulse (SET 101 or SET 010) that will be inserted in the node. Fig. 10 demonstrates this behavior in more detail for the OAI21 gate.

Table 5. Worst Radiation Sensitive Case [40]

Logic Function	Worst Radiation Sensitive Case	Complex Gate	Multi-level
OAI21	Critical Node	OUT	OUT
	Input Vector	001	011
	Transient Pulse	1-0-1	0-1-0
OAI22	Critical Node	OUT	OUT
	Input Vector	1001	0101
	Transient Pulse	0-1-0	0-1-0
AOI211	Critical Node	OUT	OUT
	Input Vector	0000	0101
	Transient Pulse	1-0-1	0-1-0
XOR	Critical Node	OUT	OUT
	Input Vector	11	11
	Transient Pulse	0-1-0	0-1-0

5.1 SET evaluation under the ideal fabrication process

The worst-case propagation delays of the four logic functions in the two topologies, considering the ideal fabrication process, are shown in Table 6. In addition to presenting some differences in performance between the use of complex and multi-level topologies, the propagation times are necessary to obtain the LETth.

Table 6. Worst-case propagation delay at nominal conditions [40]

Logic Function	Worst-case delay (ps)	
	Complex Gate	Multi-level
OAI21	7.79	18.29
OAI22	9.63	18.48
AOI211	13.42	36.63
XOR	11.68	20.02

Fig. 11 shows the SET pulse width measured when the amplitude of this same pulse exceeds half of the nominal supply voltage. To calculate the LETth of each logic gate, it is important to note that all values of the SET pulse width shown in Fig. 11 are greater than the worst-case delays shown in Table 6, characterizing the fault in the circuit output. The SET pulse width values follow much the same behavior as the delay values. The multi-level topology presents SET pulse width about 77% larger in comparison to the complex topology. This behavior does not necessarily mean a higher sensitivity of the multi-level topology to the radiation effects. The SET pulse width considering ideal fabrication tends to be higher for the multi-level topology since the functions implemented in this transistor arrangement are slower than the same ones implemented in the

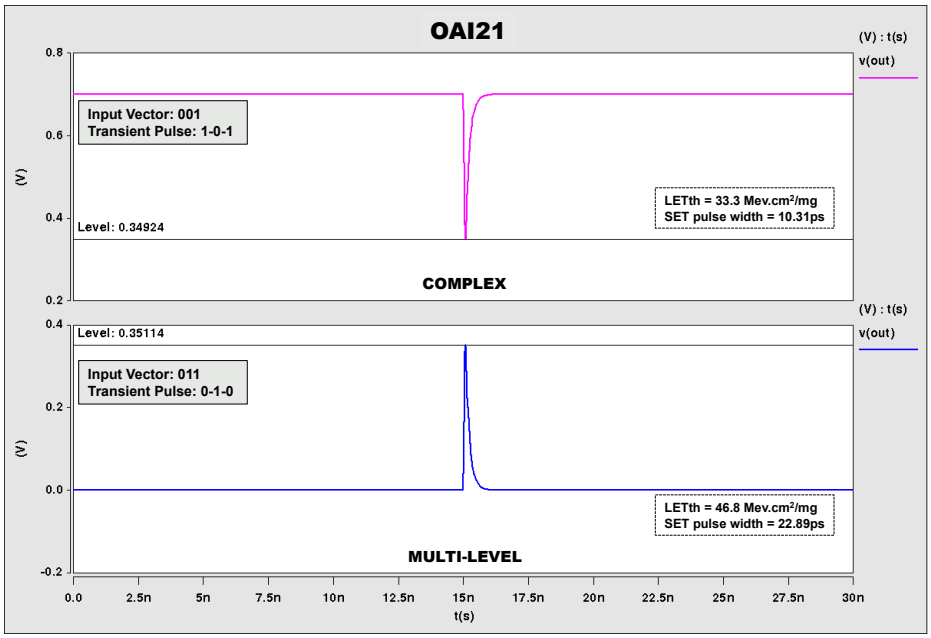


Fig. 10. The difference of transient pulse format inserted in the critical node (OUT) of complex and multi-level topologies of OAI21 gate [40].

complex topology. That is, if the SET pulse width is less than the logic gate delay, the fault would be masked.

The larger SET pulse width of the multi-level topology is not reflected in the LETth calculation, as can be seen in Table 7. LETth values may seem high considering the analyzed logic gates. However, similar work highlights the robustness of the 7nm FinFET technology, considering other logic functions [14] and also majority voter circuits [15]. NAND and NOR voters have no-fault event (at nominal supply voltage) considering a LET value of 15 Mev.cm^2/mg, for example [15]. For the OAI21 and AOI211, the LETth considering the multi-level topology is 40.54% and 72% higher than the LETth of the complex topology, respectively. XOR gate and the OAI22 gate present a difference practically null, approximately 1%. The results demonstrate that multi-level topology is more robust to the radiation effects considering the ideal fabrication process since it presents higher LETth values in comparison with complex topology. This behavior is related to the regularity of the layouts developed. The OAI22 and XOR gates, even in the complex topology, are already quite regular. Therefore, the use of multi-level topology for these functions has practically no impact.

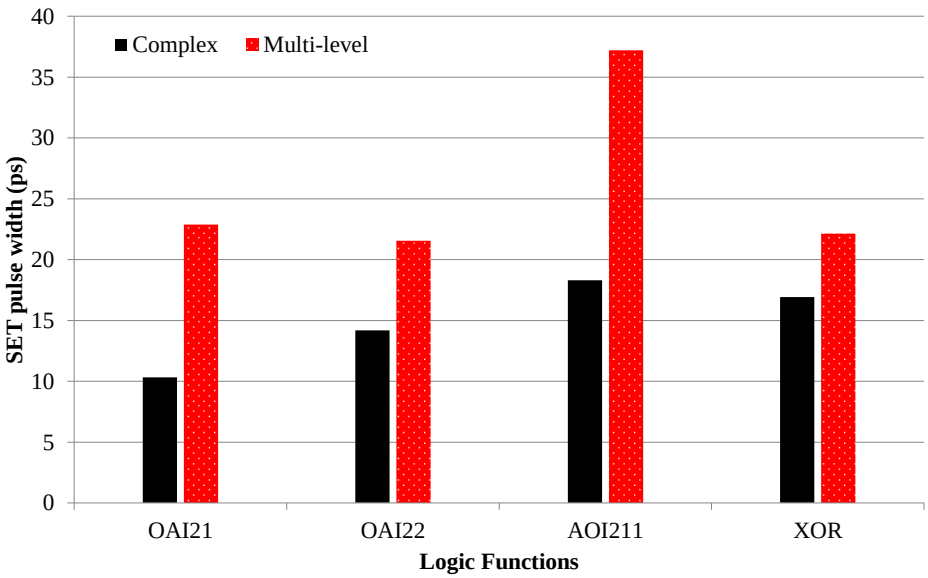


Fig. 11. SET pulse width at the ideal fabrication process [40].

Table 7. LETth at ideal conditions [40]

Logic Function	LETth (Mev.cm^2/mg)	
	Complex Gate	Multi-level
OAI21	33.3	46.8
OAI22	47.4	46.8
AOI211	27.5	47.3
XOR	46.8	46.9

5.2 The SET response under WFF

As the analysis carried out considering only the radiation effects, in the process variability analysis, the worst-case propagation delay of each logic gate is also measured but considering the WFF impact. Table 8 shows the mean (μ), standard deviation (σ) and normalized standard deviation (σ/μ) of the delays for all analyzed logic gates.

Fig. 12 shows the mean of the SET pulse width for each logic function implemented in the two topologies, considering the WFF impact. Unlike the analysis under ideal conditions, on average the SET pulse width for complex topology is higher ranging from 4ps to 9ps of difference in comparison with the multi-level topology. Only for the AOI211 gate that this ratio is not established and the SET pulse width for the multi-level topology is still about 4ps higher. Considering only the SET pulse width, the complex topology is more sensitive to the process variability effects.

Table 8. Worst-case propagation delay under WFF [40]

Logic Gates	Worst-case delay (ps)					
	Complex Gate			Multi-level		
	μ	σ	σ/μ (%)	μ	σ	σ/μ (%)
OAI21	8.43	2.56	30.37	19.21	4.00	20.83
OAI22	11.18	3.43	30.71	19.42	4.08	21.02
AOI211	14.71	4.64	31.56	38.52	7.62	19.78
XOR	12.49	2.84	22.73	20.95	4.39	20.98

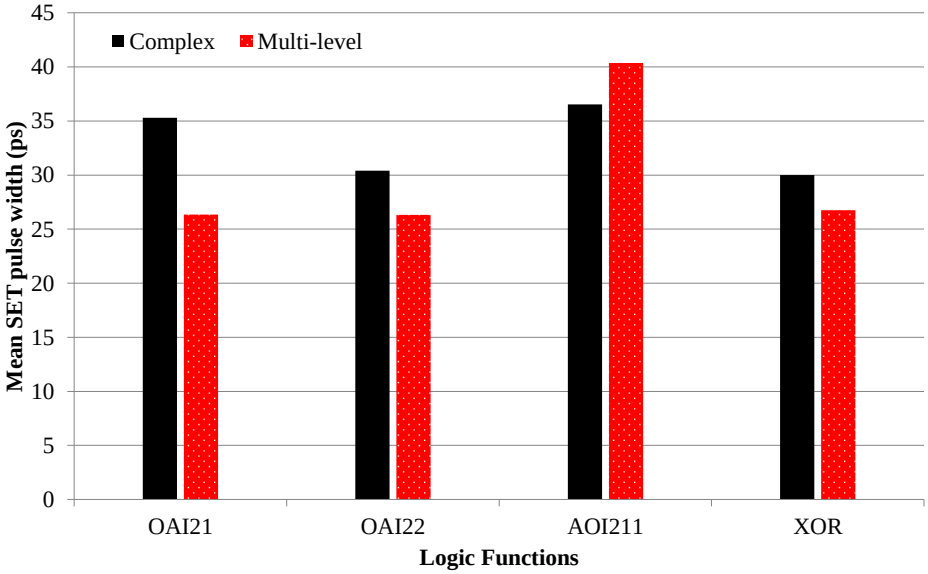


Fig. 12. Impact of WFF on SET pulse width [40].

The normalized standard deviation of the SET pulse width is shown in Fig 13. The smaller this deviation, the more robust to the variability effects is the topology used in each logic function. Although the complex topology presents higher mean values of the SET pulse width, these values deviate less than the values considering the multi-level topology for three logic functions. This difference between the deviations is not very significant, being 2.75% for the XOR gate and approximately 19% for the OAI21 gate. As in the previous analysis, for the AOI211 gate, the behavior is inverse and the multi-level topology ends up having the smallest deviation. Although the complex topology suffers from increasing the SET pulse width due to the impact of the WFF, these values have a smaller deviation than the ones considering the multi-level topology.

In the current analysis, the deviations are normalized by the mean, i.e., a smaller value of the SET pulse width means for the 2000 Monte Carlo simulations performed, tends to a more significant deviation. Still, this analysis allows

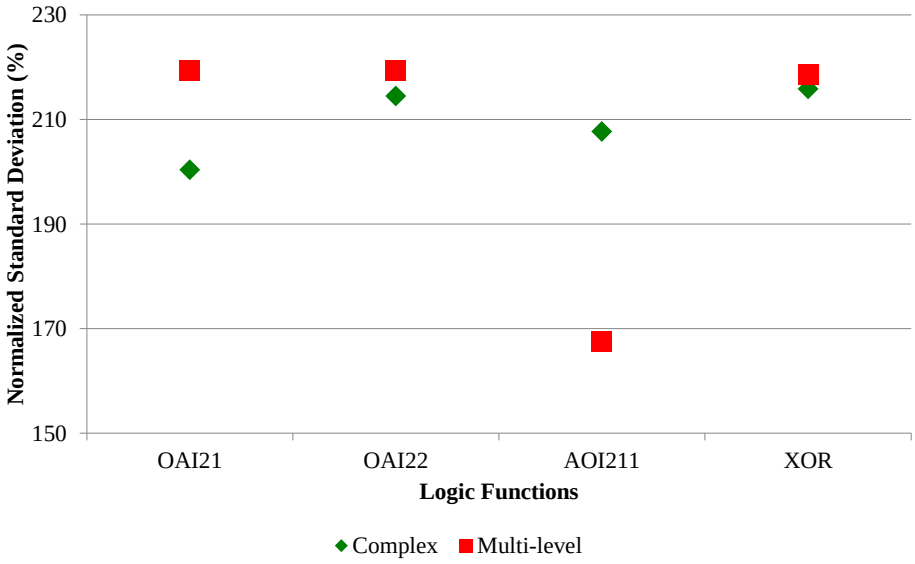


Fig. 13. Normalized standard deviation of SET pulse width [40].

observing the quantity and how much the values deviate from the mean values presented in the previous analysis. This behavior is reflected in the probability that the WFF will more or less impact the circuit. The multi-level topology has a slightly higher probability of having a SET pulse width value greater than the mean.

After obtaining the SET pulse width mean values and confirming that they are higher than the mean worst-case delay of each logic gate, the fault characterization in the circuit output is complete. Then a new LETth can be calculated considering the WFF impact. Fig. 14 shows the difference between the LETth obtained considering the ideal fabrication process and the impact of the WFF for all the logic functions in the two topologies of the study. For all logic functions regardless of the adopted topology, the LETth considering the WFF impact is smaller than the LETth at ideal fabrication process. That is, due to WFF, a smaller amount of energy transferred by the particle is required to cause a disturbance in the circuit. All evaluated circuits become more sensitive to the radiation effects. Also, in the comparison between the different transistor arrangements used in each logic gate, the multi-level topology presents the best results. For the OAI21 and AOI211 gates, the LETth considering the impact of the WFF is significantly larger in comparison with the complex topology, being 38.4% and 88% respectively. For the OAI22 and XOR gates, the LETth is smaller in the same comparison. However, signalizing a not statistically significant difference, 3.1% and 1.3%, respectively.

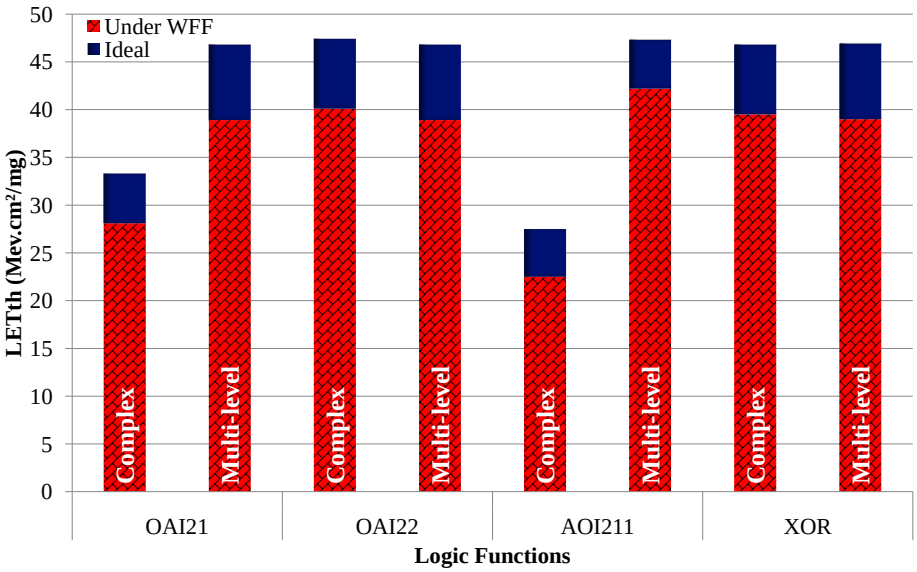


Fig. 14. Difference of LETth considering ideal fabrication process and WFF impact [40].

5.3 Area Impact

It is important to highlight one more important metric when comparing the two topologies used in this study. Table 9 shows the number of transistors and the area of each logic gate in the two topologies. All gates designed with the multi-level logic arrangement show an increase in the area used. In most cases, the area using the multi-level topology is more than three times larger than the complex gate topology. The OAI22 and AOI211 gates have the largest variation, the multi-level layout is about 4.5 times larger than the traditional layout. The XOR gate has the smallest increase in the comparison between the two topologies, approximately 67%.

Table 9. Comparison of number of transistors and area for complex gate and multi-level logic topologies

Logic	# Transistors		Area (μm^2)	
Function	Complex Gate	Multi-level	Complex Gate	Multi-level
OAI21	6	16	0.085	0.271
OAI22	8	28	0.102	0.475
AOI211	8	28	0.102	0.475
XOR	10	20	0.203	0.339

6 Conclusion

This work evaluated the radiation robustness through the SET response, considering the process variability effects. A set of logic functions implemented in two different transistor topologies was compared using the 7nm FinFET ASAP7 PDK.

Regarding the ideal fabrication process, the multi-level topology presents the largest SET pulse widths; however, it also shows the highest LETth values for three of the four analyzed logic functions. That is, at least considering the ideal fabrication, the SET pulse width has no direct relation to the LETth value. If the design objective is a more robust circuit to radiation effects, regardless of performance, power and area penalties, the multi-level topology is the best option.

Considering the process variability impact, the complex topology presents a large variation of SET pulse width values, even exceeding the multi-level topology values. Even with this variation, the LETth of the multi-level topology remains larger for two of the four logic functions and practically the same for the other two. This behavior confirms the conclusion of the previous analysis, in which the SET pulse width does not have a direct relation with the LETth value and the multi-level topology is the best option to deal with the SET effects.

The LETth values of each circuit can also be related to the environment where they will operate. On average, the LETth values of this study are around 42 Mev.cm^2/mg considering ideal conditions and around 36 Mev.cm^2/mg considering the WFF impact. Despite being high values, the logic functions are still susceptible to faults at the ground level. That is, the robustness of the this types of circuits must be considered even for applications that operate in a terrestrial environment.

In addition to the analysis of the behavior of each topology considering ideal fabrication and process variability, the impact of the WFF on the SET response was also evaluated. For all logic functions regardless of the topology used, the LETth value is lower, i.e., the logic gates become more sensitive to the radiation effects when considering the process variability impact. This analysis is of utmost importance because it indicates that to determine the LETth of a circuit, one must also consider other reliability factors such as process variability.

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References

1. Baumann, R.: The impact of technology scaling on soft error rate performance and limits to the efficacy of error correction. In: Digest. International Electron Devices Meeting,, IEEE (2002) 329–332

2. Heidel, D.F., et al.: Single-event upsets and multiple-bit upsets on a 45 nm soi sram. IEEE Transactions on Nuclear Science **56**(6) (2009) 3499–3504
3. Boudenot, J.C.: Radiation space environment. In: Radiation Effects on Embedded Systems. Springer (2007) 1–9
4. Stassinopoulos, E., Raymond, J.P.: The space radiation environment for electronics. Proceedings of the IEEE **76**(11) (1988) 1423–1442
5. Gadlage, M.J., et al.: Scaling trends in set pulse widths in sub-100 nm bulk cmos processes. IEEE Transactions on Nuclear Science **57**(6) (2010) 3336–3341
6. Auth, C., et al.: A 22nm high performance and low-power cmos technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density mim capacitors. In: Symposium on VLSI Technology (VLSIT). (June 2012) 131–132
7. Brown, A.R., Watling, J.R., Asenov, A.: Intrinsic parameter fluctuations due to random grain orientations in high-κ gate stacks. Journal of Computational Electronics **5**(4) (2006) 333–336
8. Kleeberger, V.B., Graeb, H., Schlichtmann, U.: Predicting future product performance: Modeling and evaluation of standard cells in finfet technologies. In: Proceedings of the 50th Annual Design Automation Conference, ACM (2013) 33
9. Artola, L., Hubert, G., Alioto, M.: Comparative soft error evaluation of layout cells in finfet technology. Microelectronics Reliability **54**(9-10) (2014) 2300–2305
10. El-Mamouni, F., et al.: Laser-and heavy ion-induced charge collection in bulk finfets. IEEE Transactions on Nuclear Science **58**(6) (2011) 2563–2569
11. Ferlet-Cavrois, V., Massengill, L.W., Gouker, P.: Single event transients in digital cmos—a review. IEEE Transactions on Nuclear Science **60**(3) (2013) 1767–1790
12. Artola, L., Hubert, G., Schrimpf, R.: Modeling of radiation-induced single event transients in soi finfets. In: 2013 IEEE International Reliability Physics Symposium (IRPS), IEEE (2013) SE–1
13. Meinhardt, C., Zimpeck, A.L., Reis, R.A.: Predictive evaluation of electrical characteristics of sub-22 nm finfet technologies under device geometry variations. Microelectronics Reliability **54**(9-10) (2014) 2319–2324
14. Zimpeck, A.L., Artola, L., Hubert, G., Meinhardt, C., Kastensmidt, F.L., Reis, R.: Circuit-level hardening techniques to mitigate soft errors in finfet logic gates. In: 2019 19th European Conference on Radiation and Its Effects on Components and Systems (RADECS), IEEE (2019)
15. Aguiar, Y.Q., et al.: Evaluation of radiation-induced soft error in majority voters designed in 7 nm finfet technology. Microelectronics Reliability **76** (2017) 660–664
16. Clark, L.T., et al.: Asap7: A 7-nm finfet predictive process design kit. Microelectronics Journal **53** (2016) 105–115
17. Noh, J., et al.: Study of neutron soft error rate (ser) sensitivity: investigation of upset mechanisms by comparative simulation of finfet and planar mosfet srams. IEEE Transactions on Nuclear Science **62**(4) (2015) 1642–1649
18. Sierawski, B.D., Mendenhall, M.H., Reed, R.A., Clemens, M.A., Weller, R.A., Schrimpf, R.D., Blackmore, E.W., Trinczek, M., Hitti, B., Pellish, J.A., et al.: Muon-induced single event upsets in deep-submicron technology. IEEE Transactions on Nuclear Science **57**(6) (2010) 3273–3278
19. NOAA: National geophysical data center (2015)
20. Hughes, H., McMarr, P., Alles, M., Zhang, E., Arutt, C., Doris, B., Liu, D., Southwick, R., Oldiges, P.: Total ionizing dose radiation effects on 14 nm finfet and soi utbb technologies. In: 2015 IEEE Radiation Effects Data Workshop (REDW), IEEE (2015) 1–6

21. Chatterjee, I., Zhang, E., Bhuva, B., Reed, R., Alles, M., Mahatme, N., Ball, D., Schrimpf, R., Fleetwood, D., Linten, D., et al.: Geometry dependence of total-dose effects in bulk finfets. IEEE Transactions on Nuclear Science **61**(6) (2014) 2951–2958
22. Azambuja, J.R., Kastensmidt, F., Becker, J.: Hybrid Fault Tolerance Techniques to Detect Transient Faults in Embedded Processors. Springer (2014)
23. Munteanu, D., Autran, J.L.: Modeling and simulation of single-event effects in digital devices and ics. IEEE Transactions on Nuclear science **55**(4) (2008) 1854–1878
24. Chorasia, J., Jasani, K., Shah, A.: Realization of various error mitigation techniques for sram based fpga. In: Convergence in Technology (I2CT), 2017 2nd International Conference for, IEEE (2017) 55–59
25. Bhuva, B., Tam, N., Massengill, L., Ball, D., Chatterjee, I., McCurdy, M., Alles, M.: Multi-cell soft errors at advanced technology nodes. IEEE Transactions on Nuclear Science **62**(6) (2015) 2585–2591
26. Balen, T.R.: Efeitos da radiação em dispositivos analógicos programáveis (FPAAs) e técnicas de proteção. PhD thesis, Universidade Federal do Rio Grande do Sul (2010)
27. Baumann, R.C.: Radiation-induced soft errors in advanced semiconductor technologies. IEEE Transactions on Device and materials reliability **5**(3) (2005) 305–316
28. Seifert, N., et al.: Soft error susceptibilities of 22 nm tri-gate devices. IEEE Transactions on Nuclear Science **59**(6) (2012) 2666–2673
29. Lee, S., et al.: Radiation-induced soft error rate analyses for 14 nm finfet sram devices. In: 2015 IEEE International Reliability Physics Symposium, IEEE (2015) 4B–1
30. Fang, Y.P., Oates, A.S.: Neutron-induced charge collection simulation of bulk finfet srams compared with conventional planar srams. IEEE Transactions on Device and Materials Reliability **11**(4) (2011) 551–554
31. Nassif, S.R.: Process variability at the 65nm node and beyond. In: Custom Integrated Circuits Conference, 2008. CICC 2008. IEEE, IEEE (2008) 1–8
32. Dadgour, H.F., Endo, K., De, V.K., Banerjee, K.: Grain-orientation induced work function variation in nanoscale metal-gate transistors — part ii: Implications for process, device, and circuit design. IEEE Transactions on Electron Devices **57**(10) (2010) 2515–2525
33. Topaloglu, R.O.: Design with finfets: design rules, patterns, and variability. In: Computer-Aided Design (ICCAD), 2013 IEEE/ACM International Conference on, IEEE (2013) 569–571
34. Endo, K., Matsukawa, T., Ishikawa, Y., Liu, Y., O'uchi, S., Sakamoto, K., Tsukada, J., Yamauchi, H., Masahara, M.: Variation analysis of tin finfets. In: Semiconductor Device Research Symposium, 2009. ISDRS'09. International, IEEE (2009) 1–2
35. Meinhardt, C.: Variabilidade em FinFETs. PhD thesis, Universidade Federal do Rio Grande do Sul (2014)
36. Henderson, C.L.: Failure analysis techniques for a 3d world. Microelectronics Reliability **53**(9-11) (2013) 1171–1178
37. Saha, S.K.: Modeling process variability in scaled cmos technology. IEEE Design Test of Computers **27**(2) (March 2010) 8–16
38. Brendler, L.H., Zimpeck, A.L., Meinhardt, C., Reis, R.: Evaluating the impact of process variability and radiation effects on different transistor arrangements. In: IFIP/IEEE Int. Conf. on Very Large Scale Integration (VLSI-SoC). (2018) 71–76

39. Zimpeck, A.L., et al.: Impact of different transistor arrangements on gate variability. Microelectronics Reliability **88** (2018) 111–115
40. Brendler, L.H., Zimpeck, A.L., Meinhardt, C., Reis, R.: Evaluation of set under process variability on finfet multi-level design. In: 2019 IFIP/IEEE 27th International Conference on Very Large Scale Integration (VLSI-SoC), IEEE (2019) 179–184
41. Messenger, G.: Collection of charge on junction nodes from ion tracks. IEEE Trans. on nuclear science **29**(6) (1982) 2024–2031
42. Carreno, V.A., Choi, G., Iyer, R.: Analog-digital simulation of transient-induced logic errors and upset susceptibility of an advanced control system. NASA Technical Memorandum 4241 (1990)
43. Javanainen, A., et al.: Linear energy transfer of heavy ions in silicon. IEEE Transactions on Nuclear Science **54**(4) (2007) 1158–1162
44. Hubert, G., Artola, L.: Single-event transient modeling in a 65-nm bulk cmos technology based on multi-physical approach and electrical simulations. IEEE Transactions on Nuclear Science **60**(6) (2013) 4421–4429
45. Alioto, M., Consoli, E., Palumbo, G.: Variations in nanometer cmos flip-flops: Part i—impact of process variations on timing. IEEE Transactions on Circuits and Systems I: Regular Papers **62**(8) (2015) 2035–2043