Design of a 3rd Order 1.5-Bit Continuous-Time Fully Differential Sigma-Delta (ΣΔ) Modulator Optimized for a Class D Audio Amplifier Using Differential Pairs

Nuno Pereira, João De Melo, Nuno Paulino

HAL Id: hal-01348811

https://hal.science/hal-01348811

Submitted on 25 Jul 2016

Design of a 3rd Order 1.5-bit Continuous-Time Fully Differential Sigma-Delta (ΣΔ) Modulator Optimized for a Class D Audio Amplifier Using Differential Pairs

Nuno Pereira [2], João L. A. de Melo [1,2] and Nuno Paulino [1,2]

[1] Centre for Technologies and Systems (CTS) – UNINOVA
[2] Dept. of Electrical Engineering (DEE), Universidade Nova de Lisboa (UNL)
Campus FCT/UNL, 2829-516, Caparica, Portugal
nrf.pereira@gmail.com, research@joaodemelo.com, nunop@uninova.pt

Abstract. This paper presents a 3rd order 1.5-bit Continuous-Time Fully Differential ΣΔ modulator with distributed feedback for a class D audio amplifier, using BJT differential pairs to implement the integrator stages. By relying on simple gain blocks instead of operational amplifiers to build the loop filter, a simpler overall circuit is obtained, where the non-ideal effects are embedded in the loop filter transfer function. This leads to a more difficult design process for the loop filter circuit, solved through the use of an optimization procedure based on genetic algorithms. Simulations of the electrical circuit show that it is capable of achieving a SNDR value of 73.4 dB and THD+N of about -80 dB for a signal bandwidth of 20 kHz and a sampling frequency of 1.28 MHz.

Keywords: Audio, Continuous-Time Sigma-Delta (ΣΔ), Class D Amplifier, Differential Pair.

1 Introduction

Over the years, there is a growing concern with the energy efficiency of electronic appliances, due to the global sustainability issue. Audio amplifiers are one example where the efficiency can be improved. They amplify input audio signals in order to drive output elements with suitable volume and power levels, with low distortion.

Class AB audio amplifiers have a maximum theoretical efficiency of 78.5% [1]. Class D amplifiers, due to their output power devices operating as switches, can reach an efficiency of 100% in theory. Given this fact, Class D amplifiers are the best solution in terms of efficiency for audio power amplifiers.

In order to generate the digital control signal for the power output devices of a Class D amplifier, it is necessary to convert the input analog signal into a digital signal. To do this, an Analog-to-Digital Converter (ADC) is employed. Sigma-Delta modulators (ΣΔMs) poise themselves as the best option for low frequency, high-resolution applications, given their native linearity, robust analog implementation and reduced anti-aliasing filtering requirements [2], [3].

ΣΔMs work by using negative feedback to reduce the quantization error, where a filter circuit is placed before the quantizer in order to define the frequency band where

the quantization error is attenuated. This filter is traditionally built using ideal integrator stages, which are implemented with operational amplifiers (Op-Amps) in an integrator configuration [4]-[6]. These Op-Amps require a large DC gain and bandwidth in order for the behavior of the integrator circuits to be close to the ideal integrator behavior. This can result in a complex Op-Amp circuit that is difficult to design and can dissipate a lot of power. If the ΣΔM is built using discrete components, it is also difficult to find fully differential Op-Amps as discrete components, resulting in a circuit that uses a single ended topology with all the disadvantages associated. By replacing the Op-Amps with differential pairs, it is possible to build an equivalent filter circuit for the ΣΔM using lossy integrators. The finite gain and bandwidth of the differential pairs can be accommodated during the filter design process.

This paper presents a 3rd order 1.5-bit fully differential continuous-time (CT) ΣΔM with distributed feedback for use in a Class D full-bridge audio power amplifier, where the CT integrators are based on bipolar-junction-transistor (BJT) differential pairs. Since this is a CT-ΣΔM, discrete components are used, favoring the use of BJTs over CMOS technology.

## 2   Relationship to Internet of Things

The work presented in this paper can contribute to the future development of the Internet of Things, since it can provide energy efficient communication, through the reliable transmission of information, when this information is an audio signal.

As stated in chapter I, Class D amplifiers that use ΣΔMs to transform the analog input signal into a digital signal, tend to achieve nearly 100% efficiency, while preserving linearity and providing a robust analog implementation.

A high performance can be attained through the use of ΣΔMs, since they trade speed for accuracy. This high performance is achieved with low sensitivity to analog component imperfections and without requiring component trimming [6].

3   Class D Amplifiers using Sigma-Delta Modulation

The basic block diagram of a Class D amplifier is shown in Fig. 1. The input audio signal is modulated into a digital control signal which drives the power devices in the output stage. This signal can be modulated, normally, using pulse-width modulation (PWM) or pulse-density modulation (PDM). The output stage can be implemented using a half-bridge or a full-bridge topology.
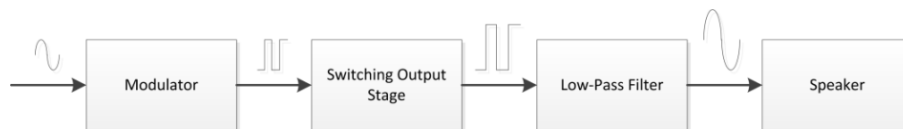
Fig. 1. Class D open-loop amplifier block diagram.

When using a ΣΔM, the digital control signal is modulated using a PDM signal. The number of pulses in a given time window is proportional to the average value of the input audio signal during that time interval. The quantization error generated in this process is averaged out, since it is fed back negatively in the ΣΔ process loop.

Class D amplifiers dissipate less power than traditional Class A/B/AB amplifiers, since the output stage devices operate as switches that alternate between the positive and negative power supplies (thus generating a train of voltage pulses). Therefore, they have zero current when in the "off" state and low voltage when conducting.

The output lowpass filter is used to remove high frequency components (that would increase the electromagnetic energy radiated by the amplifier) of the output signal, that occur due to the binary switching of the output devices.

ΣΔMs are A/D and D/A converters that operate with sampling frequencies much larger than the Nyquist frequency, trading conversion time for resolution. They are capable of increasing the signal-to-noise ratio (SNR) by filtering out quantization noise outside of the signal bandwidth. ΣΔMs are a feedback-type system, and as such, could become unstable. ΣΔMs with a maximum order of 2 are inherently stable. The stability of higher-order 1-bit modulators is of critical concern, since they include a 1-bit quantizer which only has 2 feedback levels.

# 4   3rd Order Continuous-Time ΣΔ Modulator based on Differential Pairs

When designing a ΣΔM, choosing the order and the sampling frequency are the first steps. As stated in section 3, ΣΔMs with orders higher than 2, if not designed properly, could result in an unstable system. In [8], a design procedure is presented that determines the optimal coefficients for a stable high-order ΣΔM built using ideal integrator blocks.

The goal of this paper is to design a ΣΔM optimized for an audio amplifier. A signal bandwidth of 20 kHz is chosen, since this is a standard value used for audio signals. To reduce the influence of the non-ideal effects in the output devices during the switching, a low sampling frequency must be used.

An ideal 3rd order ΣΔM (assuming that will be stable) with an oversampling ratio (OSR) value of 32 could theoretically produce a signal-to-noise-plus-distortion ratio (SNDR) value of around 95 dB. For the considered signal bandwidth, this results in a sampling frequency f_s of 1.28 MHz. However, due to the inherent instability of the modulator, the SNDR value could drop to 64 dB [8].

4.1 1.5-bit ΣΔ Modulator with Distributed Feedback and Ideal Integrators

The block diagram of a 3rd order 1.5-bit ΣΔM with distributed feedback is shown in Fig. 2. The signal transfer function (STF) and the noise transfer function (NTF) of this modulator are given by (1). As expected they are a 3rd order transfer function.
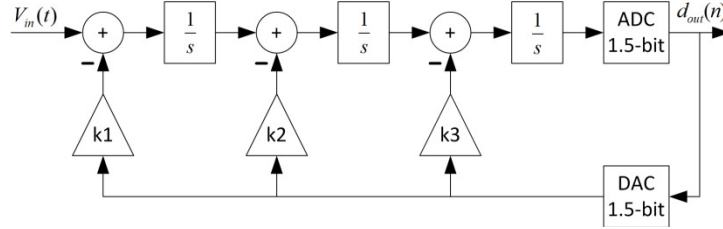
Fig. 2. Block diagram of a 3rd order 1.5-bit ΣΔM with distributed feedback.

$$STF = \frac{1}{s^3+k_3 \cdot s^2+k_2 \cdot s+k_1} \qquad NTF = \frac{s^3}{s^3+k_3 \cdot s^2+k_2 \cdot s+k_1} \qquad (1)$$

The values of the coefficients k_1, k_2 and k_3 are determined, through numeric computing software (e. g. *MATLAB*®), in order to implement the desired filtering function e. g. a Butterworth filter. The cut-off frequency of the filter is selected as a trade-off between stability of the modulator (lower cut-off frequency value) and increased SNDR value of the modulator (larger cut-off frequency value) [8].

By using a 1.5-bit quantizer (3 levels) instead of a 1-bit quantizer (2 levels), the linearity of the feedback path in the modulator is improved. This results in a more stable loop and in a decrease of unnecessary switching of the output stage. This will lead to a higher SNDR value than what would be obtained if a 3rd order 1-bit ΣΔM was used.

4.2   Integrating Differential Pairs

An inherent advantage of differential pairs is that they are a fully-differential circuit. Due to its symmetry, the differential output voltage of this circuit does not depend on the input common-mode voltage, leading to a high common-mode rejection ratio (CMRR). However, although the output is independent from the input common-mode voltage, the differential pair transistors must be biased to operate in the active region. This imposes limits to the input common-mode range [9]. If exceeded, the circuit will present nonlinearities, leading to distortion.

Differential pairs have an advantage that results from their symmetry: even order harmonics tend to be cancelled, since even order terms are canceled. Thus, the quality of the circuit will be determined by the third order harmonic (and subsequent odd harmonics). The basic building block for the ΣΔM will be the integrating differential pair circuit presented in Fig. 3. The supply voltages used were of ± 5V.

Both capacitors $C_{1,2}$ perform the integration operation, while resistors $R_{C1,2}$ define both the gain and the output common mode DC voltage, set in this circuit to 2.5 V (half of the positive supply voltage), to ensure that following integrator stages and their BJT are properly biased. Feedback resistors $R_{fb1,2}$ add the output signal to the input signal (V_{in}). Both input resistors ($R_{b1,2}$) limit the voltage applied to the base of the BJT, ensuring that it is low enough to prevent saturation. The biasing current source, I_{EE}, is implemented by a basic current mirror.
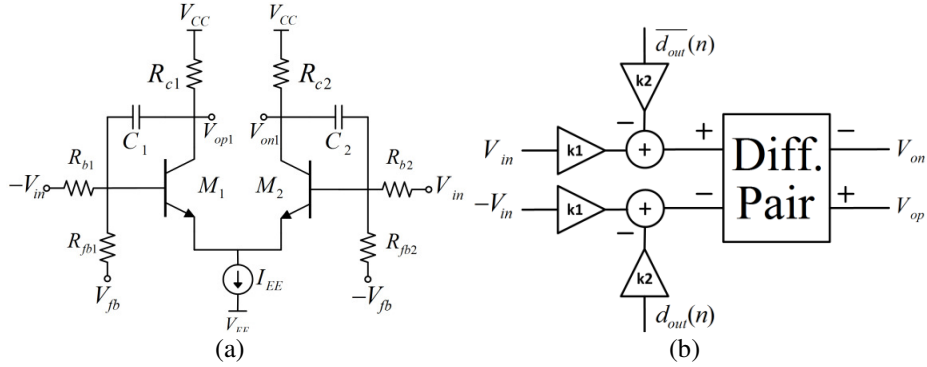
Fig. 3. Schematic of the integrator Differential Pair (NPN) (a) and Symbolic View (b).

Using the Kirchhoff's current law (KCL) applied to the small signal model; it is possible to obtain the output differential voltage equation of this circuit (2).

$$V_{out} = \frac{2R_c(V_{fb}R_b - V_{in}R_{fb})(sC_{int}r_\pi - \beta)}{R_{fb}r_\pi(1 + sC_{int}R_c) + R_b\left(r_\pi + sC_{int}R_c r_\pi + R_{fb}\left(1 + sC_{int}(\beta R_C + R_c + r_\pi)\right)\right)} \tag{2}$$

Capacitors C_1 and C_2 behave like Miller capacitors, introducing an additional zero to the circuit. Since the sampling frequency value is low, this zero does not cause a problem because its value is much larger than f_s.

The common-mode output voltage of the circuit is larger (2.5 V) than the common mode input voltage (0 V). Therefore, it is necessary to use a complementary version of the circuit in Fig. 3 based on PNP transistors. This complementary circuit has a common mode input voltage of 2.5 V and a common mode output voltage of 0 V. Thus, a PNP integrator stage should be preceded by a NPN integrator stage and followed by another NPN integrator stage and so forth.

In order to reduce distortion in the circuit, the signal amplitude at the base of each BJT should be small (below 50 mV [9]) to ensure that no transistor saturates (thus reducing distortion). This condition must be met during the filter design process, using available degrees of freedom from the design variables.

4.3   1.5-bit ADC

To achieve 1.5-bit quantization (three levels), the integrator output voltages must be compared with a certain threshold voltage ($\Delta V_o - V_t > 0$). Since the design in question is fully-differential, the circuit in Fig. 4 was used in order to avoid using many comparators. The threshold voltage is generated through a voltage divider between the V_o voltages and two reference voltages (here denoted as $V_R{}^{+,-}$). The logic codification of the 1.5-bit quantizer is shown next to the 1.5-bit ADC (Fig. 4). The equation that represents this ADC is given by (3).

$$\Delta V_t = \Delta V_o \frac{R_2}{R_1 + R_2} - \Delta V_R \frac{R_1}{R_1 + R_2} \tag{3}$$

Rearranging the right side of (3), it follows that,

$$\frac{R_2}{R_1+R_2}\left(\Delta V_o - \Delta V_R \frac{R_1}{R_2}\right) \tag{4}$$

which is similar to $\Delta V_o - V_t$. Thus,

$$\Delta V_R \frac{R_1}{R_2} = V_t \tag{5}$$

From (5), it is possible to obtain the relation between R_1 and R_2, for a given V_t, $V_R{}^+$ and $V_R{}^-$. This V_t voltage is determined through simulations of the proposed architecture in order to obtain the optimum SNDR value.

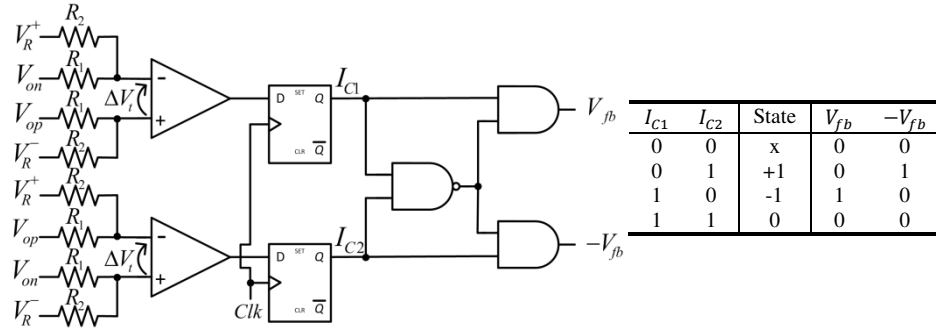| I_{C1}	I_{C2}	State	V_{fb}	$-V_{fb}$
0	0	x	0	0
0	1	+1	0	1
1	0	-1	1	0
1	1	0	0	0

Fig. 4. Fully Differential 1.5 bit ADC.

4.4 Filter Design

For a 3rd order $\Sigma\Delta$M, three integrator stages are used, resulting in the circuit of Fig. 5. The denominator of the transfer function of this architecture will be similar to the one in Eq. (1). The transfer function of the circuit is very complex and impossible to be fully presented in this paper. By equating this denominator to the coefficients obtained when designing the 3rd order Butterworth filter with a certain cut-off frequency, it is possible to obtain the optimal values for the feedback resistors ($R_{fb1,2}$). In order to do so, some component values have to be assumed, like the capacitors and the R_b resistors.
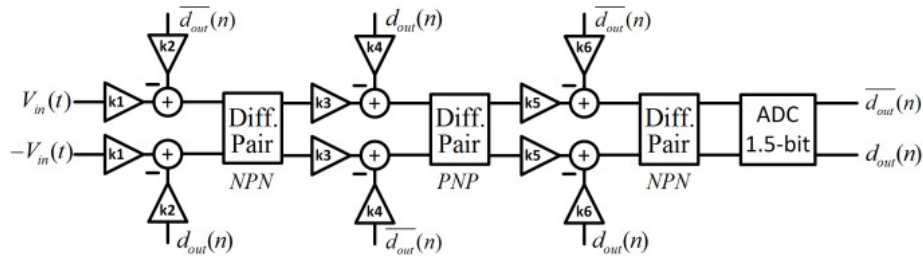

Fig. 5. 3rd Order 1.5-bit CT Fully Differential $\Sigma\Delta$M implementation.

Although fairly accurate, this is a long and time-consuming method. So, the sizing of the 3rd order ΣΔM was performed through the use of a genetic algorithm, proposed in [10], where quantization noise, voltage swing variations and stability of the modulator are taken into account. This sizing also considers sensitivity to component variations. The values for the components of the circuit obtained after the sizing process are shown next in Table I, the biasing current is 5 mA. The reference voltages of the 1.5-bit ADC ($V_R{}^+$ and $V_R{}^-$) are +5 V and -5 V respectively.

TABLE I.   COMPONENT VALUES

Component	Value	Units
$C_{1,2} = C_{3,4} = C_{5,6}$	0.47	nF
$R_{b1,2}$	42.136	kΩ
$R_{b3,4}$	1.227	kΩ
$R_{b5,6}$	3.741	kΩ
$R_{fb1,2}$	67.634	kΩ
$R_{fb3,4}$	24.673	kΩ
$R_{fb5,6}$	27.694	kΩ
$R_{c1,2} = R_{c5,6}$	1	kΩ
$R_{c3,4}$	3	kΩ
R_1	54	Ω
R_2	5	kΩ

5   Simulations & Results

Fig. 5 shows the circuit implementation of the proposed architecture and its sizing is shown in Table I. Electrical simulations of the complete circuit were performed for different input amplitudes. The resulting output spectrum for an input signal of 1 V (0.707 V$_{rms}$) is shown in Fig. 6 (a) and the SNDR as a function of the input voltage is plotted in Fig. 6 (b).

(a)   (b)
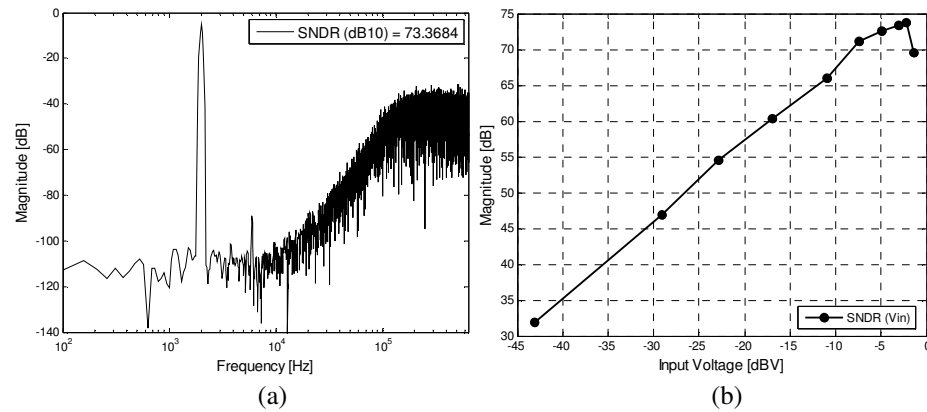
Fig. 6. Output spectrum of the architecture (Blackman-Harris window with 2^{16} points) (a) and obtained SNDR as a function of the input voltage (dBV) (b).

The electrical simulation results show that for a signal bandwidth of 20 kHz and a sampling frequency of 1.28 MHz, a maximum SNDR value of 73.4 dB was obtained. The Total Harmonic Distortion plus noise (THD+N) obtained is about -80 dB.

6   Conclusions

This paper presented a 3rd order 1.5-bit CT Fully Differential ΣΔM, where the integrators that compose the circuit were realized through basic BJT differential pairs, against traditional Op-Amp methodology that is more costly.

When compared to ΣΔMs implemented with Op-Amps, this architecture can reach a similar performance and this poses as an improvement, since cheaper circuits can be used while designing a more efficient circuit.

Simulation results of the electrical circuit show that a SNDR of 73.4 dB is obtained, for a signal bandwidth of 20 kHz and a sampling frequency of 1.28 MHz.

References

1. Sedra, A. S., Smith, K. C.: Microelectronic Circuits. Oxford University Press, USA, (2003)
2. Carusone, T. C.: Analog Integrated Circuit Design. Wiley (2011)
3. Schreier, R., Temes, G. C.: Understanding Delta-Sigma Data Converters. John Wiley & Sons (2004)
4. Yan, S., Sanchez-Sinencio, E.: A continuous-time sigma-delta modulator with 88-dB dynamic range and 1.1-MHz signal bandwidth. In: IEEE Journal of Solid-State Circuits, vol. 39, n. 1, pp. 75 - 86 (2004)
5. Wu, R., Long J. R., van de Gevel M., Glassche G.: A fifth-order continuous-time sigma-delta modulator with 62-dB dynamic range and 2MHz bandwidth. In: Research in Microelectronics and Electronics Conference, 2007. PRIME 2007. Ph.D, pp. 17 -20 (2007)
6. de Melo, J., Paulino N: Design of a 3rd order 1.5-bit continuous-time (CT) Sigma-Delta (SD) modulator optimized for Class D audio power amplifier. J. Microelectronics and Computer Science, vol. 1, no. 2 (2011)
7. Brigati, S., Francesconi, F., Malcovati, P., Tonietto, D., Baschirotto, A., Maloberti, F.: Modeling sigma-delta modulator non-idealities in SIMULINK(R). In: Proceedings of the 1999 IEEE International Symposium on Circuits and Systems, 1999. ISCAS '99, vol. 2, pp. 384 -387 vol.2 (1999)
8. Norsworthy, S. R., Schreier, R., Temes, G. C.: Delta-Sigma Data Converters: Theory, Design, and Simulation. 1st ed. Wiley-IEEE Press (1996)
9. de M. Silva, M.: Circuitos com transistores bipolares e MOS. Fundação Calouste Gulbenkian (2003)
10. de Melo, J. L. A., Nowacki, B., Paulino, N., Goes, J.: Design methodology for sigma-delta modulators based on a genetic algorithm using hybrid cost functions. In: Proc. IEEE Int. Symp. Circuits Systems (ISCAS'12), pp. 301-304 (2012)