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Abstract. This paper presents a full-bridge discrete power output stage for a Class D audio amplifier using a single-ended power supply. The circuit receives a digital control signal with 5 V of amplitude and it generates a floating differential output voltage up to 20 V of amplitude from a single 20 V power supply voltage. Using as control signal a pulse density modulation (PDM) wave generated by an optimized 3rd order continuous-time (CT) sigma delta modulator (ΣΔM), the system achieves a signal-to-noise-plus-distortion ratio (SNDR) of 83.1 dB, total harmonic distortion (THD) of -89 dB and a power efficiency of 92 %, while delivering 11 W over an 8-Ω load with a signal bandwidth of 20 kHz and a sampling frequency of 1.28 MHz.

Keywords: Class D Audio Amplifier, Output Stage, Gate Driver.

1 Introduction

There has been an ongoing tendency to increase the energy efficiency of every electronic device as global sustainability starts to be a major concern. Audio amplifiers are not different as they play a big role regarding power consuming in electronic systems. In Class D amplifiers the output stage devices operate as switches, resulting that when the CMOS output transistors are conducting there is a small drain-to-source voltage drop causing the dissipated power by them to be close to zero. Comparing with the typical Class AB amplifier, which has a maximum theoretical efficiency of 78.5 %, the Class D amplifier can theoretically achieve a power efficiency of 100 % [1].

The performance of a Class D audio amplifier output stage is mainly determined by the output stage configuration and the quality of the output switching [2]. The full-bridge configuration versus the half-bridge configuration can cancel out even order harmonic distortion, DC offset, allows the use of a single power supply (which doubles the available power supply voltage) and the use of a 1.5-bit quantization scheme. This quantization scheme will provide current to the load only when needed, decreasing the switching activity thus causing the power efficiency to increase while decreasing the electromagnetic interference (EMI) [3]-[4]. The output power

transistors connect the output nodes either to the positive power supply or ground, therefore it is important to guaranty that they do not conduct simultaneously, in order to prevent large current spikes from the positive power supply to ground from occurring. This results in a need to introduce non-overlapping time which is called *dead time* in the control signals and is one of the most dominant sources of distortion in Class D audio amplifiers [6]. In general, in a Class D output stage, the power output transistors are implemented using two identical NMOS transistors in a totem-pole configuration. These are preferred due to their small area and capacitance. Nonetheless, in order to drive the high side NMOS power transistor it is necessary additional circuitry using more complicated techniques (e.g. bootstrap technique) and timed circuitries in order to correctly activate the necessary transistors [7]-[9].

The proposed output stage presented in this paper, depicted in Fig. 1, relies on a full-bridge configuration and in a PMOS-NMOS output totem-pole arrangement which enables the high side gate driver to have a simpler circuitry. The goal is to achieve a THD close to -90 dB (0.0032 %) and power efficiency higher than 90% while using a single 20 V power supply over an 8-Ω load.

The system behavior is as follows. The analog input signal is modulated into a digital signal through pulse-width modulation (PWM) or pulse-density modulation (PDM), then this signal is level-shifted in order to drive the output CMOS power transistors and finally the differential output voltage is filtered by a low-pass filter, which reconstructs the signal before the loudspeaker in order to eliminate the high frequency content. The non-overlapping time module provides the necessary time delay in order to prevent simultaneous conduction between the output transistors. The modulation part of the system has a feedback from the output stage which enables the system to correct the output stage errors and to increase the power supply rejection ratio.

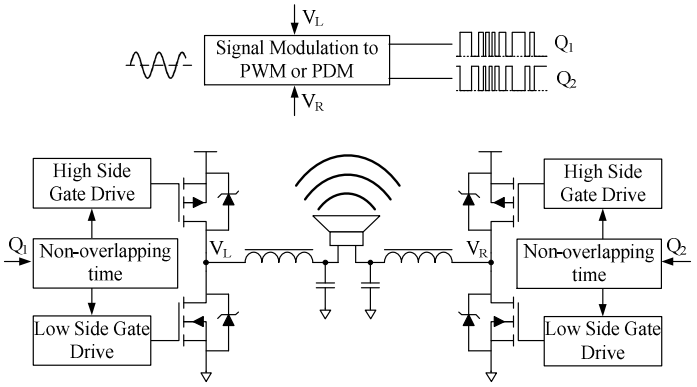

Fig. 1. Class D audio amplifier with full-bridge configuration.

2 Relationship to Internet of Things

The Internet of Things refers to uniquely identify objects and their virtual representations in an Internet-like structure. If all objects and people in daily life were

equipped with radio tags, they could be easily identified and inventoried by computers. In a social context, audio amplifiers, especially Class D amplifiers, being high efficiency are able to aid visual conditioned people in their day-to-day living by identifying the object/person as they come by with an extended life battery.

3 Class D Audio Amplifiers Output Stage

3.1 Low Side Gate Driver

The power output NMOS transistor gate can be simply driven by a CMOS inverter. Controlling the inverter switching with timed pulses can significantly decrease the power consumption. Fig. 2(a) shows the proposed low side driver and Fig. 2(b) shows the simulated voltages and currents in the circuit.

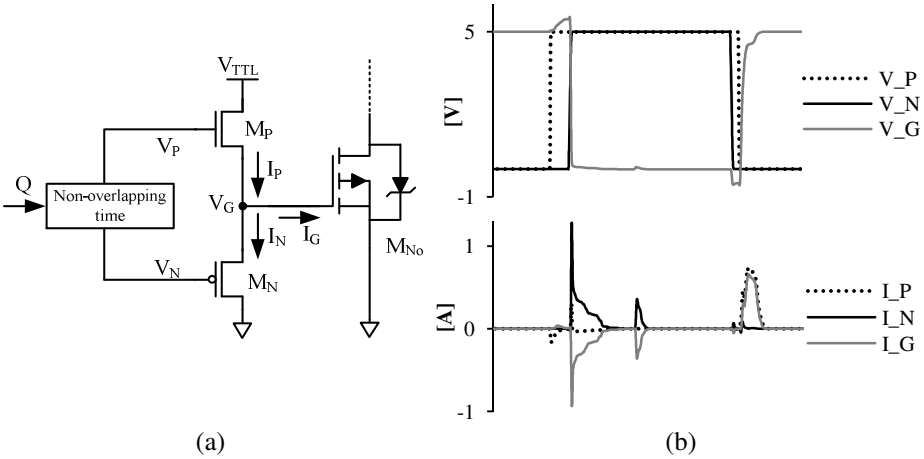

Fig. 2. (a) Low side gate driver and power NMOS transistor (b) Simulated voltage levels and current flow in the low side gate driver during the M_{N0} switching.

In order to achieve high efficiency the drain current of M_P (I_P) and M_N (I_N) should only flow to the gate of M_{N0} (I_G). This can be achieved by using the correct non-overlapping value, as represented in Fig. 2(b). Otherwise, a large current can flow from the power supply through the inverter (M_P and M_N).

3.2 High Side Gate Driver

The starting point for this circuit was the PMOS gate driver described in [10] and depicted in the box of Fig. 3(a). The circuit operation is as follows: when P_1 is high the transistors M_1 and M_2 are on, forcing the base-to-emitter voltage drop of transistor Q_1 to be zero, turning it off. M_2 will also push-down the gate voltage of transistor

M_{PLeft} to zero, turning it on. When P_1 is low, the transistor Q_1 will turn on due to the resistor R_1 which will pull-up the gate voltage of M_{PLeft}.

This means that the M_{PLeft} turn-off speed is dependent on R_1 which imposes a severe trade-off: when M_{PLeft} is on, a DC current $V_{CC}/(R_1+R_{DS(M1)})$ will flow through R_1 and M_1, creating an undesired power dissipation. Increasing R_1 in order to reduce this current will slow down the M_{PLeft} turn-off speed as this resistor bias Q_1. This classifies the gate drive as Class A when the M_{PLeft} is off, as it is necessary to have a constant DC current.

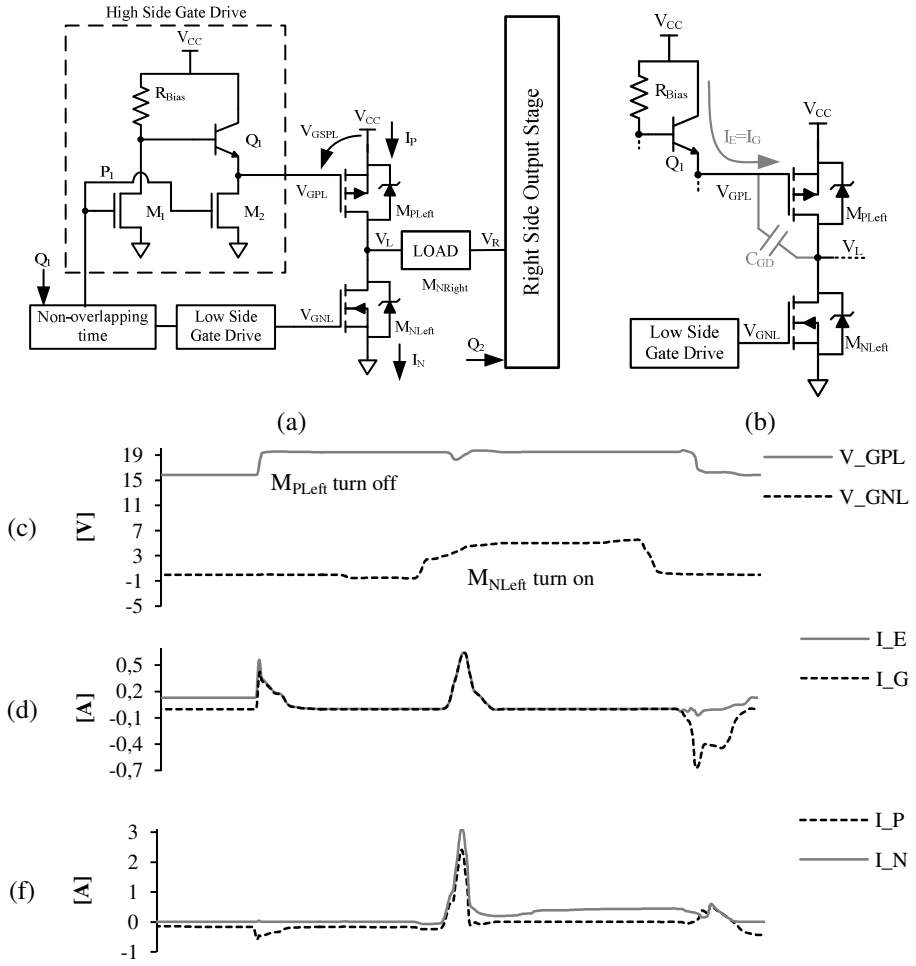

Fig. 3. (a) PMOS gate driver [10] (in box) in full-bridge configuration (b) PMOS gate driver [10] representation with parasitic capacitance while M_{NLeft} turn on and an example showing the simulated (c) V_{GPL} and V_{GNL} voltages (d) I_E and I_G currents (f) I_P and I_N currents.

By inspecting the circuit it is possible to see that the M_{PLeft} gate-to-source voltage, V_{GSPL}, during M_{PLeft} turn-off, is equal to $V_{RBias}+V_{BE(Q1)}$. This means that M_{PLeft} is not

fully turned off as V_{GSPL} is not exactly zero. Fig. 3(b) shows the high side gate driver with parasitic capacitances during the M_{PLeft} turn off and M_{NLeft} turn on, and on Fig. 3(c), (d) and (f) an example with the simulated transitory waves is also shown. As M_{PLeft} is turning off, V_{GPL} value increases to V_{CC} - V_{R1}+V_{BE} which in the shown example is 19.5 V, with a 20 V power supply. After the non-overlapping time the V_{GNL} voltage increases to 5 V turning M_{NLeft} on. This will pull down the node V_L, forcing the V_{GPL} node also to be pulled down, due to the parasitic capacitance C_{GD} of M_{PLeft} being large (as represented in Fig. 3(b)). This will cause the V_{GSPL} voltage to increase, falsely turning M_{PLeft} on and creating large current spikes between V_{CC} and ground through transistors M_{PLeft} and M_{NLeft} because they are simultaneously conducting. This effect is called *shoot-through current* [5] and will decrease the efficiency significantly, introduce harmonic distortion and even destroy the output transistors if Q_1 takes too long to respond to this variation.

This problem is bypassed by the proposed high side gate driver presented in this paper.

3.3 Proposed High Side Gate Driver

The new full-bridge output stage proposed in this paper is presented in Fig. 4. Two CMOS inverters were placed at the gate of the output PMOS. In order to achieve lower power dissipation, especially in R_{Bias}, one zener diode was inserted in each branch of the circuit. The zener voltage of these diodes should be V_{CC} – 5 V so that the V_{GS} voltage drop of the output PMOS transistor, the R_{Bias} voltage drop and the CMOS inverters only varies from 5 V to V_{CC}. This will cause the V_{GS} voltage drop of the PMOS to be constant thus improving the performance of the circuit while simplifying the voltage supply scaling, as only the zener diode needs to be scaled.

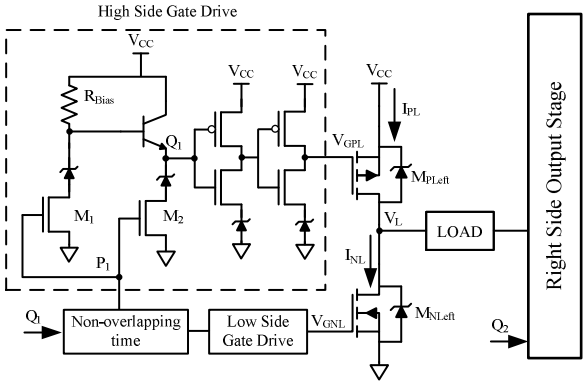

Fig. 4. Proposed PMOS gate driver (in box) in full-bridge configuration.

The inverters placed at the gate of the output PMOS will correctly pull-up V_{GPL} to V_{CC} so that it will be correctly turned off. The correctly timed delay will prevent shoot-through current.

An example for the switching waves of the output stage is shown on Fig. 5. The circle in Fig. 5(b) shows a commonly found effect in Class D output stages. As V_L voltage rises to V_{CC}, a parasitic current goes from V_{CC} through the parasitic capacitance C_{GD} of the NMOS power transistor. This effect is rapidly compensated by the low side gate driver.

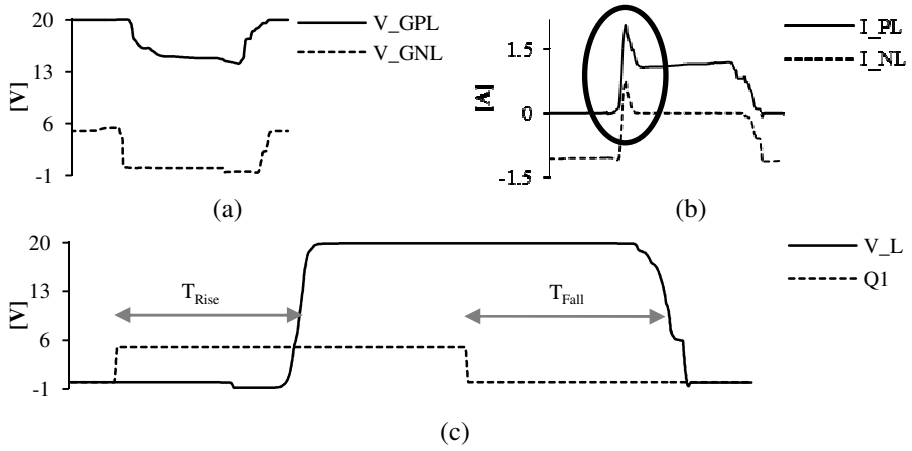

Fig. 5. Simulated example for (a) switching voltage levels at the gate of the output power transistors (b) current in the output power transistors (c) input voltage (Q_1) and output voltage (V_L) with the T_{Rise} and T_{Fall} delay represented.

4 Class D Audio Amplifier with a 3rd Order 1.5-bit Continuous-Time (CT) Sigma Delta (ΣΔ) Modulator

The presented output stage was simulated with a 3rd order 1.5 bit ΣΔM optimized for Class D audio amplifiers with distributed feedback and local resonator feedback, described in [11]. The output stage was design to handle 20 V power supply, 20 kHz low-pass filter, a sampling frequency of 1.28 MHz and to drive an 8-Ω load.

Fig. 6(a) shows the P_{RBias} dissipation plot during continuous conduction and the Fig. 6(b) shows the T_{Rise} and T_{Fall} delay of the output stage with the R_{Bias} increase. From these plots it is possible to conclude that the output stage power efficiency will increase as R_{Bias} increases, but the ΣΔM will have to handle the output stage increased delay. The used 3rd order ΣΔM was optimized using 100 ns and 150 ns delay while using the same goal function. This allowed the use of R_{Bias} values between 60 to 100 Ω and 160 to 200 Ω, respectively. Table 1 shows the system performance summary for these optimizations and Fig. 7 shows the fast Fourier transform (FFT) of the output sinusoidal wave while applying a 0 dBV and 2 kHz input signal.

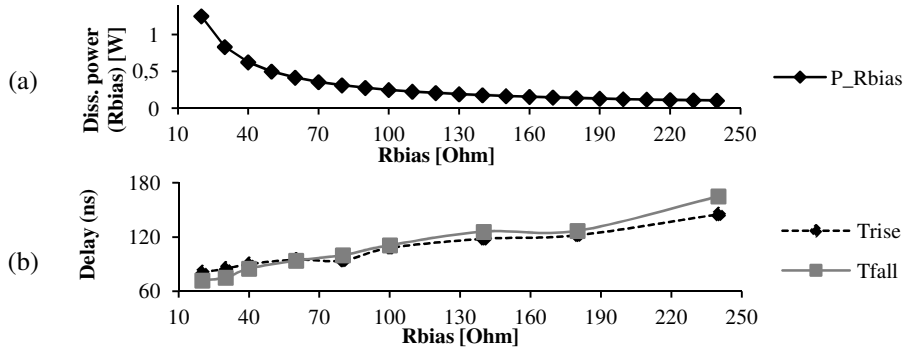

Fig. 6. (a) P_{Rbias} plot ($P_{Rbias} = 5^2/R_{Bias}$) (b) T_{Rise} and T_{Fall} delay.

Table 1. System performance summary with 100 ns output stage delay optimization (#1) and 150 ns delay optimization (#2)

Optm.	R_{Bias} (Ω)	SNDR (dB)	THD (dB)	HD2 (dB)	HD3 (dB)	η (%)	P_{Load} (W)	Delay (ns)	
								Up	Down
	60	82.21	-84.96	-90.3	-89.3	87.90	13.36	100	95
#1	80	81.92	-84.76	-90.8	-88.8	89.21	13.36	105	100
	100	83.09	-86.38	-93.1	-89.2	89.76	13.36	113	110
	160	83.62	-89.70	-98.4	-101.5	91.73	11.29	125	135
#2	180	83.41	-87.08	-97.1	-100.4	91.69	11.30	135	140
	200	83.14	-88.94	-99.9	-106.3	92.20	11.30	140	150

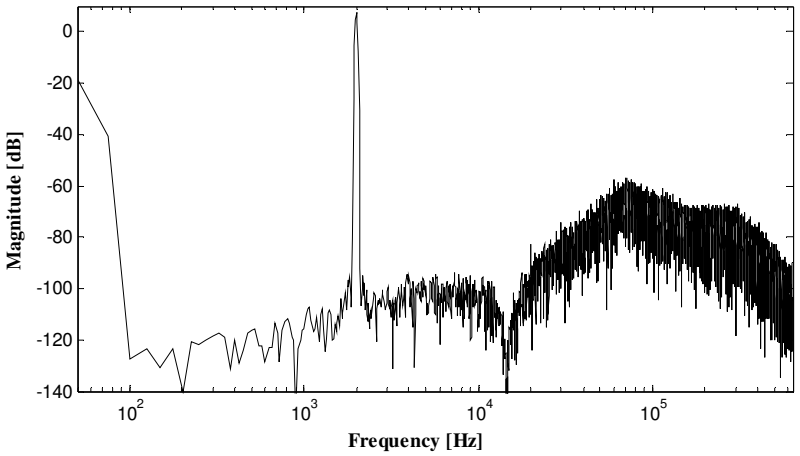

Fig. 7. Spectrum of the output signal (using a Blackman-Harris window and 2^{16} points) with R_{Bias} equal to 200 Ω and SNDR of 83 dB.

These results show that using a higher R_{Bias} value the system will operate with higher power efficiency, higher SNDR and lower harmonic distortion, but will deliver less energy to the output load. This is due to the increased T_{Rise} and T_{Fall} delay which

will result in a smaller active time in the output PDM wave, thus reducing the maximum output power. The best compromise between SNDR, harmonic distortion and power efficiency has been found to be with R_{Bias} equal to 200 Ω where the system achieves a SNDR of 83 dB, THD of -89 dB and power efficiency ($P_{Load}/P_{delivered}$) of 92%.

5 Conclusions

A full-bridge discrete power output stage for a Class D audio amplifier using a single 20 V power supply voltage was presented. The circuit is controlled by a digital 5 V of amplitude PDM signal, produced by an optimized 3rd order ∑Δ modulator with the output stage inside the closed loop. This system is capable of driving an 8-Ω load while achieving a SNDR of 83 dB and a THD of -89 dB (0.0035 %). The use of a PMOS-NMOS power output inverter simplified the design while still achieving power efficiency of 92% for an 11.3 W power delivered to the load. The use of 1.5-bit quantization scheme and the lossless LC low-pass filter allowed to reduce the EMI distortion (max. of -60 dB at 80 kHz).

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