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Abstract. The continuing size reduction of electronic devices imposes design challenges to optimize the performances of modern electronic systems, such as: wireless services, telecom and mobile computing. Fortunately, those design challenges can be overcome thanks to the development of Electronic Design Automation (EDA) tools. In the analog, mixed signal and radio-frequency (AMS/RF) domains, circuit optimization tools have demonstrated their usefulness in addressing design problems taking into account downscaling technological aspects. Recent advances in EDA have shown that the simulation-based sizing technique is a very interesting solution to the 'complex' modelling task in the circuit design optimization problem. In this paper we propose a multi-objective simulation-based optimization tool. A CMOS LC-VCO circuit is presented to show the viability of this tool. The tool is used to generate the Pareto front linking two conflicting objectives, namely the VCO Phase Noise and Power Consumption. The accuracy of the results is checked against HSPICE/RF simulations.

Keywords: Multi-Objective Optimization, Metaheuristic, Pareto Front, Simulation-based optimization, LC-VCO, Inductor 2-π model.

1 Introduction

Analog, mixed signal and radio-frequency (AMS/RF) circuit design are becoming more and more complex; there is a pressing need for Electronic Design Automation (EDA) to meet the time to market constraints. Indeed, automation in circuit design has successfully demonstrated its usefulness, from circuit level design, see for instance [1–4], to system level designs, see for example [5–8]. The current computers features have favoured a transition from the hand-calculation-based design, to the simulation-based design. The first, which is known as the knowledge-based design, is one of the earlier approaches. Its basic idea is to have a predefined design plan for sizing circuits to meet the performance specifications [9–11]. The second one, i.e. the simulation-based approach, is based on the use of a circuit simulator such as SPICE, which evaluates the circuit's performance(s) and constraints, as well [12–14]. The key of

this transition is the feasibility to include SPICE like simulators within the loop of any circuit design optimization problem.

The simulation-based approach is adopted in this work. This technique uses a standard circuit simulator in the optimization loop to evaluate the circuit performance. In this way, this approach can handle a large variety of AMS/RF circuits. Among the advantages of this method, it offers a great accuracy at the expense of design time while an analytical approach is faster but suffers from accuracy limitations.

Actually, AMS/RF circuit optimization problems generally involve more than one objective. These objective functions are conflicting and non-commensurable ones. A multi-objective metaheuristic is used in this work to efficiently find the optimum design of an LC voltage controlled oscillator (LC-VCO).

The main concerns in this design are the passive elements, principally the inductor.

When implementing an on-chip inductor, the influence on circuit behaviour that come up from inductor parasitics are usually ignored and the inductor is considered as an 'ideal' element. Yet, this is a wrong approach, since at high frequencies the parasitic capacitances that appear between metal layers and oxide/substrate can have significant weight and jeopardize the expected inductance value.

Despite the fact that the simulation-based technique is accurate and that the obtained results are precisely those of the simulator (since the component simulator models are adopted), at high frequencies, parasitics effects of passive components (mainly inductors) can not be neglected: using the ideal models of these components is a common mistake.

In this work we deal with inductor parasitics and use the proposed tool to size the circuit and the inductor, as well, since classical sizing approaches cannot be used for such design due to its complexity.

For the inductor the 2-π model [15-16] is used in the in-loop optimisation simulation based tool in order to highlight potentialities and performances of the proposed tool and to show the real effect of parasitics of inductors. An LC-VCO circuit is considered as an application example.

The rest of the paper is structured as follows. In section 2, we clearly show the main contributions of this work. In section 3, we put the light on the proposed tool and highlight its capabilities. In section 4, we present the multi-objective optimization. In section 5, the LC-VCO circuit, which includes the inductor equivalent circuit, is used to validate the optimization tool. Finally, conclusions are offered in section 6.

2 Relationship to Internet of Things

Internet of things relies on the interconnections of a large number of heterogeneous cooperating devices. The development of these devices has been made possible due to the rapid evolution of electronic technologies, which enable the implementation of ever more complex functions, in smaller and more rapid circuits. To cope with the necessity of minimizing the power consumption of such systems, new design methodologies must be adopted so that the ever more stringent specifications may be attained. In the particular case of communications services, e.g. wireless

communications devices, Voltage Controlled Oscillators (VCOs) are fundamental building blocks where optimization design methodologies must be adopted to cope with such multi-objective design goals, e.g. low power consumption and low phase noise.

The contributions of this paper are as follows:

- A multi-objective simulation based tool that allows generation the Pareto front of conflicting objectives of analog and RF circuits, is proposed;
- The use of the 2-π model for the electrical simulation of the inductor in the loop-optimization. By using a lumped element model, an efficient process is obtained, thus overcoming the need for using lengthy electromagnetic simulations of the inductor.

3 The Simulation-Based Sizing Tool

As introduced in Section 1, the simulation-based optimization technique is adopted in order to be able to deal with complex circuits. Its basic idea consists of 'by-passing' the modelling stage in the sizing problem and to directly use an electrical simulator to evaluate the objective functions, and to check the circuit's constraints, as well. In each optimization iteration the circuit simulator is called to evaluate the circuit's performance(s) for a set of design parameters. A pictorial diagram of this approach is presented in Figure 1 [14].

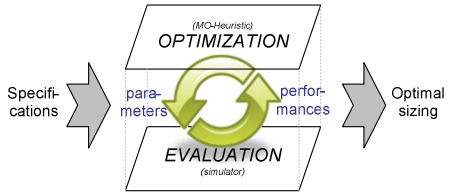


Fig. 1. The simulation-based sizing/optimizing technique [14].

One of the key components in this technique is the optimization block, whose purpose is to find the best circuit's sizing that will lead to the best performance while satisfying a set of constraints. In this work, we use a multi-objective metaheuristic called MOHA [17]. This algorithm is based on a communication tool between HSPICE/RF and C++ software.

In short, this tool works as follows. After generating the circuit's netlist, the parameters' values are introduced in this netlist. Then, the C++ program calls HSPICE/RF thanks to which, constraints are checked and performances are evaluated. These performances are then introduced in the optimization algorithm and 'new' sizes are generated, etc.

In order to deal with multi-objective problems, an external archive was added to the optimization routine [17] where non-dominated solutions are stored and updated at each iteration. A dominance sorting routine [18] was integrated into the optimization program. This external memory encompasses the 'best' non-dominated solutions obtained so far. It is to be mentioned that these performance evaluations are

performed using the simulator .MEAS statement which prints user-defined electrical specifications of a circuit, and the results could be manipulated in a post-processing step. Figure 2 shows the corresponding algorithm flowchart. Further details regarding MOHA can be found in [17].

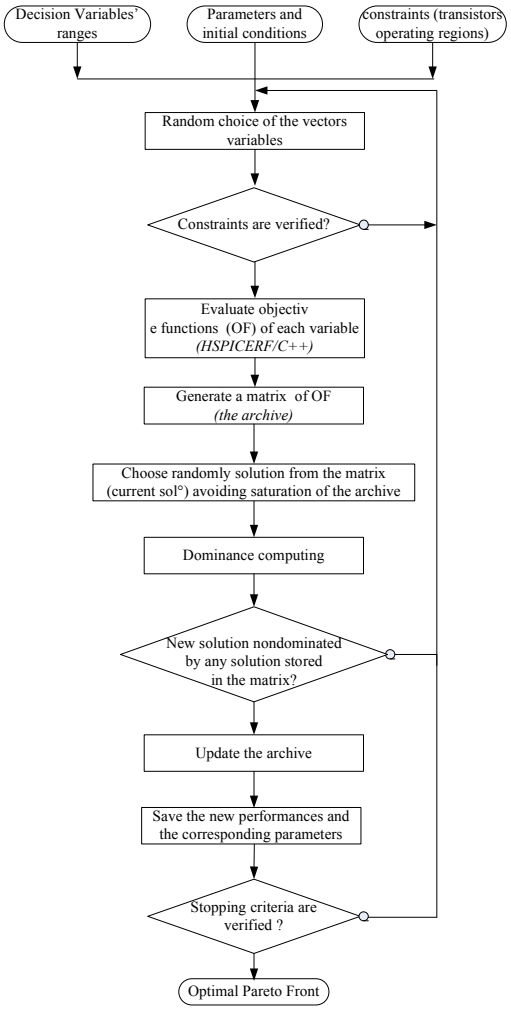


Fig. 2. Flowchart of MOHA.

4 The Multi-Objective Optimization

Actually, circuit optimization problems involve more than one objective function that meets all the performance functions and imposed/inherent constraints. In most cases,

the considered sizing problems are multi-objective ones. Equation (1) illustrates this multi-objective optimization (MOO) problem:

$$\begin{cases} Minimize\ \vec{f}(\vec{x}); & \vec{f}(\vec{x}) \in R^{k} \\ subject\ to: & \\ \vec{g}(\vec{x}) \le 0; & \vec{g}(\vec{x}) \in R^{m} \\ and\ \vec{h}(\vec{x}) = 0; & \vec{h}(\vec{x}) \in R^{n} \\ where\ x_{Li} \le x_i \le x_{Ui}, & i \in [1, p] \end{cases} \quad (1)$$

where, k, m, n and p are the numbers of objectives ($k \geq 2$), inequality constraints to satisfy, equality constraints to assure and parameters to manage respectively.

Commonly, designers transform the multi-objective problem into a mono-objective one using the weighting technique [19]. The latter requires the designer to select values of weights for each objective. The so obtained mono-objective function can be written as:

$$F(\vec{x}) = \sum_{i=1}^{k} \omega_i f_i(\vec{x}) \quad (2)$$

ω_i are weighting coefficients.

However, it has been proven that this technique is not suitable and may lead to non-optimal solutions (see for instance [20]).

Due to the fact that in most cases, circuits present conflicting non-commensurable objectives, making appeal to the multi-objective techniques is mandatory. Actually, such techniques allow generating the aforementioned sets of non-dominated[1] solutions known as Pareto fronts [18].

In the literature, a large plethora of multi-objective metaheuristic were/are being used, to optimize performances of AMS/RF circuits (mainly using the equation-based approach) [2–4, 8, 21–22].

In this work we use a multi-objective metaheuristic, called *Multi-Objective Heuristic Algorithm* (MOHA) [17].

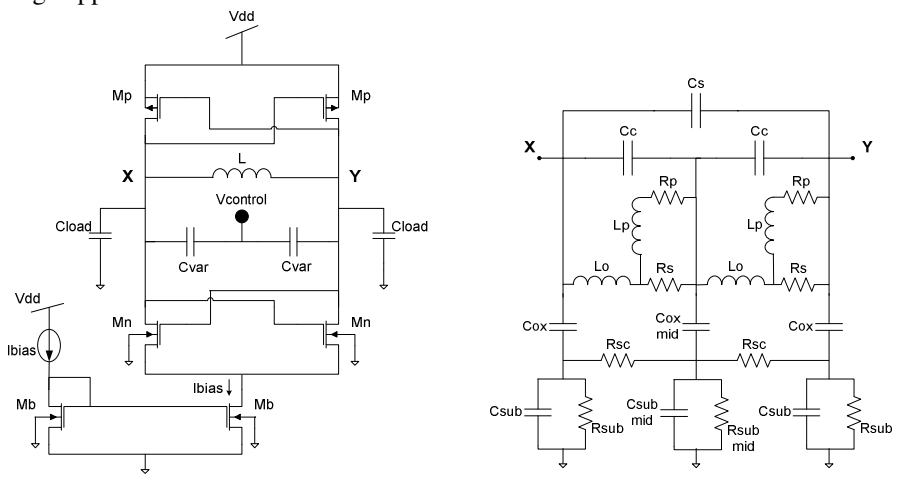
5 Application to the Optimal Design of an LC-VCO Circuit

5.1 The LC-VCO Equivalent Circuit

One of the main challenges when designing a VCO, is to obtain results between simulation and on-chip measurement as close as possible. For this propose, it is essential to use design methodologies where parasitics must be accounted for, even when simulators are used. In Fig. 3(a) a cross-coupled LC-VCO is represented. It

[1] A solution $\vec{x}$ of a MO problem is said non-dominated solution if and only if there does not exist another solution $\vec{y}$ such that $\vec{f}(\vec{y})$ dominates $\vec{f}(\vec{x})$, i.e. no component of $\vec{f}(\vec{x})$ is smaller than the corresponding component of $\vec{f}(\vec{y})$ and at least one component is greater.

encompasses two main blocks: the LC thank, responsible for the oscillation frequency, and the active circuit, which accounts for reducing the circuit losses by introducing a negative resistance. The transistor *Mb* is responsible for enforcing the current in the circuit. Most LC-VCO designs aim at achieving both minimum phase noise and power consumption for a given oscillation frequency. For instance, if low power consumption is desired, a low bias current must be delivered to the circuit. Yet, parasitic effects will have a major role in circuit behaviour, yielding to the degradation of phase noise. On the other hand, if low phase noise is required, high current is desired. The phase noise *vs* power consumption trade-off, among others, makes the VCO design a suitable applicant for simulation-based optimization based design approach.



(a) The cross coupled topology (b) The inductor equivalent circuit

Fig. 3. LC – voltage controlled oscillator (LC-VCO).

As mentioned before, the LC tank is the block responsible for the oscillation frequency, and plays a major role in the LC-VCO performance. Since inductor parasitics appearing between the inductor metal tracks and the lower layers of oxide and substrate are very relevant for GHz frequencies, an inductor equivalent circuit model, known as 2-π inductor model [15], represented in Fig. 3(b), is considered. The inductor 2-π equivalent circuit. This inductor equivalent model accounts for:

- DC parameters (L_o, L_p, R_s, R_p);
- Crossover capacitance, *Cs* - that capacitance appears between the spiral and the underpass necessary to connect the inner turn to the outside of the spiral inductor;
- Metal-to-metal capacitance, *Cc* – that appears due to the proximity of inductor tracks;
- Metal-to-substrate capacitance, C_{ox};
- R_{sub} and C_{sub} that models the ohmic losses in the conductive silicon substrate;
- R_{sc} which represents the electric coupling between lines through the conductive substrate.

5.2 Simulations Results

In this section the design of several LC-VCOs for operating frequencies between 1 and 2 GHz, are addressed. The design objective functions are the minimization of both the phase noise - @ an offset frequency of 1MHz - and the power consumption. The LC-VCO characteristics and 2-π inductor circuit parameters range are given in Table 1, where the transistor channel length/width range is valid for *Mp*, *Mn* and *Mb* elements. Moreover, the capacitor *Cvar* is in fact a transistor that behaves as a capacitor (referred as MCvar in Table 2), and its channel length/width range is considered to be equal to *Mp*.

Table 1. LC-VCO and 2-π inductor circuit parameters limit

LC-VCO circuit	Oscillation frequency - f_0	1 GHz – 2 GHz
	Transistor channel length	0.45 µm – 1.6 µm
	Transistor channel width	1 µm – 500 µm
	Tank inductance - L	1 nH – 15 nH
	Tank capacitance - C_{var}	1 pF – 20 pF
	Load capacitor C_{Load}	2 pF
2-π inductor circuit	Cs, Cc, Csub, Csub_mid	0.1 pF – 20 pF
	Cox, Cox_mid	0.1 fF – 1 pF
	Lo, Lp	0.01 nH – 10 nH
	Rs	0.01 Ω – 30 Ω
	Rp	1 Ω – 1 kΩ
	Rsc, Rsub, Rsub_mid	10 kΩ – 10 MΩ

In Fig. 4 we present the two Pareto fronts (*Phase Noise vs. Power*) obtained using the proposed tool for two different scenarios: considering ideal and real inductors. The supply voltage is V_{DD} = 1.2 V and the voltage at the gate of the transistor *Mb* is equal to 0.4V. Simulations are performed using Level 49 standard CMOS Technology of 0.13µm. As expected optimization results considering ideal inductors are quite better than those with real inductors. By simple observation, it is possible to conclude that for a specific phase noise, the power consumption for the LC-VCO considering a real inductor is higher by a factor of 8. That means that results obtained for ideal inductors are too optimistic.

Reached performances and optimal parameter values corresponding to the Pareto front edge points of MOHA algorithm are in Table 2 and 3: solutions giving the maximum phase noise and the minimum power, solutions (1) and (2) in figure 4 respectively. Considering the design solution (1) in Table 2, the inductance of the inductor equivalent circuit is 3.8 nH. Now, if a simulation is done for the same transistors sizes, but considering an ideal inductor of 3.8 nH, the LC-VCO characteristics are: 1.18 mW, 2.04 GHz and -122.87 dB/Hz. These results show an error around 15% for power, 6% for the oscillation frequency and 4% for the phase noise when compared with those obtained with the inductor equivalent circuit.

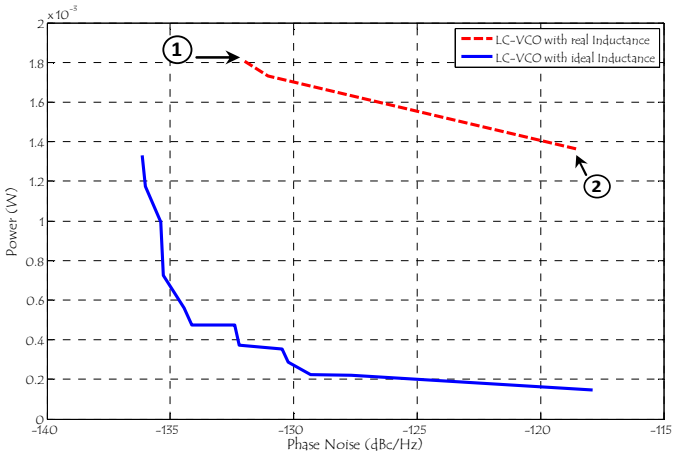


Fig. 4. LC-VCO optimization results Pareto fronts (Phase Noise vs. Power consumption).

Table 2. Optimal parameters values (LC-VCO with real inductor)

Parameters	***Lower edge of the Pareto front (solution(2))***	***Higher edge of the Pareto front (solution(1))***
Mp – width / length (µm)	176.75 / 1.57	273.75 / 0.63
Mn – width / length (µm)	256.75 / 1.57	190.25 / 0.63
Mb – width / length (µm)	240.75 / 1.57	489.25 / 0.63
MCvar – width / length (µm)	472.75 / 1.57	80.25 / 1.15
Inductance (nH)	0.62	3.83

Table 3. Reached performances (points located at the Pareto front edges)

		Lower edge of the Pareto front (solution(2))	***Higher edge of the Pareto front (solution(1))***
Real Inductor	***Phase Noise (dBc/Hz)***	-118.49	-131.99
	Power Consumption (mW)	1.36	1.80
	Oscillation Frequency (GHz)	1.94	1.45
Ideal Inductor	***Phase Noise (dBc/Hz)***	-117.87	-136.15
	Power Consumption (mW)	0.14	1.32
	Oscillation Frequency (GHz)	1.17	1.02

6 Conclusions

A multi-objective simulation based tool that allows generation the Pareto front of conflicting objectives of analog and RF circuits, is proposed. As a proof of concept, the work addressed the design of LC-VCOs as a simulation-based sizing problem.

The methodology presented deals with the complexity of the design by formulating it as a multi-objective metaheuristic optimization problem. The adoption of the 2-π model of the inductor and its use in the electrical simulation-based optimization loop, aims to obtain design solutions in which simulations are expected to be close to those in fabricated circuits.

The use of multi-objective optimization strategy, allows dealing with design trade-offs, such as power consumption - phase noise, obtaining the best design solution, supported on designers inputs.

A set of design examples showing the design of LC-VCOs for oscillation frequencies between 1 and 2 GHz is shown. The presented results highlight the differences in circuit performance when using circuits that characterize the real device behaviour rather than ideal ones, as shown for the inductor.

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