# Adaptive Logical Control of RF LNA performances for efficient energy consumption

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# Adaptive Logical Control of RF LNA Performances for Efficient Energy Consumption

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**Abstract.** This work presents a new approach for controlling power consumption in RF devices. The approach is based on the definition of application-dependent performance modes for power hungry RF circuits and a logical control strategy that adjusts the power supply of each circuit to the mode required by the application. The control strategy uses embedded sensors, a recursive parameter identification approach and regression models for performance prediction, while demanding minimum embedded resources for computation. The control strategy is robust with respect to circuit parametric deviations due to the manufacturing process or ageing mechanisms. The strategy is illustrated for the case of an RF LNA using envelop detectors as embedded sensors. Simulation results of the control strategy at the transistor-level illustrate the energy savings that can be obtained for an example application.

**Key words:** Control, parameter identification, ARX models, recursive least squares method, regression, RF transceivers

## 1 Introduction

An efficient management of energy consumption is of paramount importance for battery-operated wireless devices. The autonomy and life span of these devices directly depends on procedures aimed at saving energy. The total power consumption is largely determined by the radio frequency (RF) front-end, in particular the power amplifier (PA) and the low noise amplifier (LNA) that are found, respectively, in the transmission and reception paths. Achieving high energy efficiency for these components, while maintaining a high degree of linearity, has been a major issue in low power wireless communications from a hardware design standpoint [1]. Energy savings can also be obtained using a software-based control. Most typically, energy hungry components are switched off during idle times.

In this work, we will study further energy savings that can be obtained by considering different performance modes for each RF circuit and controlling the required power supply. Each performance mode of a Circuit Under Control (CUC) has a different power consumption associated with it. The sequence and time duration of performance modes must be scheduled by the underlying application or by demand from the communication network. The implementation of such an approach is not straightforward. A major challenge is to guarantee the performance level during each CUC mode by just controlling the power supply during all the operational life of the device. In fact, for each CUC, parameter variability, ageing mechanisms and operation disturbances can make difficult to guarantee the required performance level while only power supply is controlled.

For this, we propose a closed loop logical control scheme to adjust the power consumption of an RF CUC according to the required performance mode. Since the CUC performances are not directly available for measurement, the controller must estimate them, regardless of the RF input and output signals of the CUC. The control algorithm compares the estimated performances with the target performances of the desired mode, and acts accordingly on the CUC power supply. The controller takes as input the signals coming from embedded sensors placed at the CUC input and output. These signals are used in a recursive real-time parameter identification algorithm to extract the coefficients of the input/output behavioural model. Regression functions stored in the controller map the behavioural model coefficients to CUC performances.

The rest of this work is organised as follows. Section 2 briefly reviews recent works on control, parameter identification and performance prediction for mixed-signal/RF integrated devices. Section 3 describes the models used by the controller for parameter identification and performance prediction. The on-line parameter identification procedure and the logical control strategy are described in Section 4. Section 5 describes a case-study RF LNA and the embedded sensors. An analytical study of the variation of LNA performances with the power supply is given and suitable performance modes for this circuit are identified. Section 6 presents simulation results at the transistor level of the logical control approach. Finally, some conclusions and directions for future work are given in Section 7.

## 2 Related works

Integrated devices in nanometer technologies are highly susceptible to parametric deviations of the fabrication process, variations of the power supply, environmental disturbances and ageing effects. To address these problems, there is a rapidly growing interest on digitally-assisted analog design where digital logic is used to compensate for loss of mixed-signal/RF performance [2].

On-line parameter identification techniques have recently been considered for calibration and test of mixed-signal/RF circuits using recursive algorithms. For example, [3] uses a Sign-Data Least Mean Square (SD-LMS) algorithm for the calibration and test of a pipeline converter. The technique uses a reference

ADC, which has high accuracy but low speed, in parallel with the pipeline ADC under test that operates at high speed but with less accuracy. The input analog signal is sampled and converted by both ADCs. A calibration block implements a recursive SD-LMS algorithm that takes as input the output of the pipeline ADC and the sign of the error committed between both ADCs. The output of the calibration block is a digital correction signal applied to the pipeline ADC in order to minimize the error.

The use of on-line parameter estimation of linear systems from binary data has partially been addressed in [4]. Nonlinear control for improving RF PA efficiency and linearity has been considered in [5]. The use of autoregressive models and parameter identification for analog test and diagnosis has been considered in [6, 7].

A different paradigm for on-line test and tuning of RF systems has been introduced in [9, 10]. The performances of the CUC are estimated using regression functions. These functions are obtained through Multi-variate Adaptive Regression Splines (MARS) and they are implemented in a Digital Signal Processor (DSP). The input for these functions is provided via embedded sensors that are placed in specific circuit nodes. The sensors extract characteristic device features that are used by the DSP in the regression-based performance prediction for testing [9] or tuning [10] purposes. In a recent work, [8] considers the tuning of RF performances using digital signatures. The Hamming distance between the reference signature and the actual signature is used to control the device, without the need of performance prediction from the observed responses. A set of possible operating levels is defined. At each iteration of the control algorithm, the device changes from one level of operation to another while minimizing the Hamming distance of the digital signature.

The novelty of our work stems from, firstly, a new procedure that uses both on-line recursive least mean square (LMS) parameter identification and regression functions for performance estimation and, secondly, the application of this procedure for efficient energy consumption in RF circuits for which different performance modes can be defined. Through signal converters for power supply control and sensor response measurement, we demonstrate a logical control algorithm that requires minimum digital resources for computation.

## 3 Model building

The models required for the online logical control of a CUC must be computed at the design stage. These models include:

- a behavioural input/output model of the CUC, and
- a nonlinear model that links the set of parameters in the behavioural model to the performances of the CUC.

Figure 1 illustrates the procedure for the construction of these models. Monte Carlo simulation of N samples of the CUC (which includes the embedded sensors) is considered. For each sample $i$, the set of performances $P_i$ are calculated

by simulation. In addition, a transient simulation of the CUC is also carried with a persistently exciting input sequence $u(k)$ that covers the frequency range of the CUC. This is typically a Gaussian stimulus up converted to the CUC central frequency. The output sequence $y_i(k)$ is obtained via the embedded sensor, typically an envelop detector. For the set of N CUC samples, we obtain the set of performances $\mathbf{P} = \{P_1, \ldots, P_N\}$ and the set of output transient sequences $\mathbf{Y} = \{y_1(k), \ldots, y_N(k)\}$. For a given model structure with $m$ parameters, an identification algorithm uses the input sequence $u(k)$ and the resulting set of output sequences $\mathbf{Y}$ to estimate the set of behavioural model parameters $\mathbf{\Theta} = \{\Theta_1, \ldots, \Theta_N\}$, where $\Theta_i = \{\theta_i^1, \ldots, \theta_i^m\}$ corresponds to the set of $m$ behavioural parameters for the i-th sample. Finally, from the set of performances $\mathbf{P}$ and the set of behavioural model parameters $\mathbf{\Theta}$, nonlinear regression is used to compute a performance prediction model.

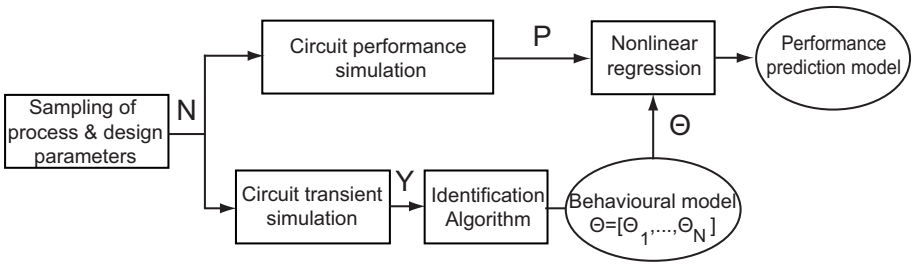



**Fig. 1.** Model building during the design phase.

In Figure 1, the structure of the behavioural model for the identification algorithm is known a priori. In practice, the structure of this model may be obtained after several iterations until the most accurate prediction models are obtained.

### 3.1 Behavioural input/output model

Behavioural modelling aims to find a mathematical relationship between the input/output transient sequences of the CUC. In this work we will use autoregressive models, so that the input/output relationship of the $i^{th}$ sample is expressed as

$$y_i(k) = f(\gamma_i(k), \Theta_i), \tag{1}$$

$$\gamma_i(k) = [y_i(k-1), \ldots, y_i(k-n_y), u(k-1), \ldots, u(k-n_u)]. \tag{2}$$

where $\gamma_i(k)$ defines first order regressors that consider the memory of the model. It contains $n_u$ previous values of $u(k)$ and $n_y$ previous values of $y_i(k)$. $\Theta_i$ is the parameter vector of the model. In most practical cases, the behavioural model is

nonlinear with respect to the parameters. In this work, a priori knowledge of the CUC (e.g. an LNA) allows us to restrict the study to dynamic models that are linear with respect to the parameters and function $f(.)$ has a polynomial form.

To find the model structure, we apply the identification algorithm indicated in Figure 2. Some algorithm constants are fixed by the user according to his a priori knowledge of the CUC. These include the maximum memory allowed for the input sequence $u(k)$ and the output sequence $y(k)$, respectively, $n_{u-max}$ and $n_{y-max}$. Also, since the model can be nonlinear with respect to the input, the maximum powers that can be applied for the input values $u(k-j)$ and output values $y(k-j)$ in the expression of the polynomial function $f(.)$, respectively, $p_u$ and $p_y$, are also given as constants. The model structure of the $i^{th}$ CUC sample will now contain higher order regressors given by Equation 3:

$$\gamma_i(k) = [u(k-1), \ldots, u(k-n_{u-max}), \ldots, u(k-1)^{p_u}, \ldots, u(k-n_{u-max})^{p_u}, \\ y_i(k-1), \ldots, y_i(k-n_{y-max})^{p_y}]. \quad (3)$$

The algorithm searches a model structure that contains regressors constructed from these variables. Each regressor has a weight $w_j$ associated with it. These weights are used in the objective function to penalize or encourage the corresponding regressor. They are proportional to the memory and the exponential power of the variables in the regressor.

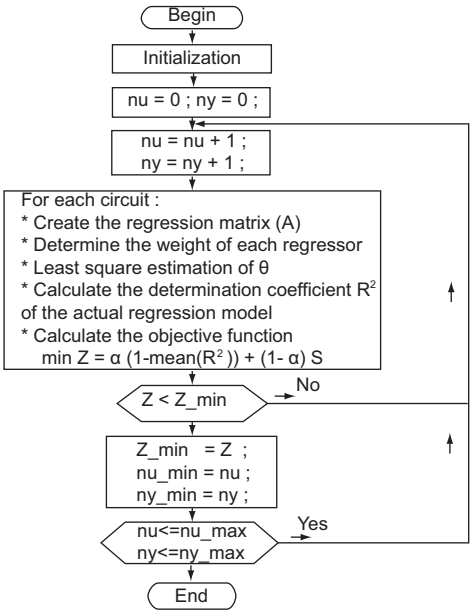



**Fig. 2.** Identification algorithm for deriving an input/output model structure

The identification algorithm is based on LMS estimation of the parameter vector $\Theta_i$ of the behavioural model, that is, the value of $\Theta_i$ that minimises the regression error $\varepsilon_i$ in

$$Y_i = A_i \Theta_i + \varepsilon_i, \tag{4}$$

where

$$Y_i = \begin{pmatrix} y_i(k-1) \\ \vdots \\ y_i(k-n_{max}) \end{pmatrix} \tag{5}$$

is the output sequence of length $n_{max}$ of the $i^{th}$ sample of the CUC, $n_{max} = max\{n_{u-max}, n_{y-max}\}$ and

$$A_i = \begin{pmatrix} \gamma_i^T(k) \\ \vdots \\ \gamma_i^T(n_{max}+1) \end{pmatrix} \tag{6}$$

is the regression matrix composed of vectors of the form of Equation 3, which are monomial terms of polynomial $f(.)$ in Equation 2.

The LMS estimation of $\Theta_i$ is given by

$$\hat{\Theta}_i = (A_i^T A_i)^{-1} A_i^T Y_i. \tag{7}$$

The quality of the regression is quantified by the determination coefficient $R_i^2$, given by

$$R_i^2 = 1 - \frac{\varepsilon_i^T \varepsilon_i}{\sum_k (y_i(k) - \overline{y_i})^2}. \tag{8}$$

Finally, a multi-objective cost function is used in the identification algorithm to select the most suitable model structure. This function is given by

$$Z = \alpha(1 - \frac{1}{m} \sum_{i=1}^{m} R_i^2) + (1-\alpha)S, \tag{9}$$

where $\alpha$ is a weighting factor for the two criteria of the objective function. $S$ is a criterion used to penalize the complexity of the behavioural model structure as follows

$$S = \frac{\sum_{j \in selected-model} w_j}{\sum_{l \in full-model} w_l}, \tag{10}$$

where the numerator corresponds to the sum of the weighting factors of the regressors in the selected model, and the denominator to the sum of the weighting factors in a full model that contains all possible regressors.

### 3.2 Nonlinear performance prediction model

Nonlinear regression is performed to obtain a relationship between each performance in the set $\mathbf{P}$ of CUC performances, and the set $\mathbf{\Theta}$ of estimated parameter

vectors as shown in Figure 1. Simple functions are required in order to minimise the computation resources required on-chip. For this, we use a kind of Branch and Bound algorithm to explore a predefined space of regressors. These regressors use as variables the coefficients $\mathbf{\Theta}$ of the model structure. The predefined space is limited to second order polynomial regressors. The steps of this algorithm for obtaining the regression functions for each performance are as follows:

- Circuit data ($\mathbf{P}$,$\mathbf{\Theta}$) are randomly separated into training and validation sets.
- The complete space of regressors is considered to form a reference regression matrix. Each column of this matrix corresponds to a regressor that is weighted according to its complexity given by the sum of the power of the involved variables. An initial value of predicted performances is obtained using the best correlated column of this matrix with the performance we want to predict.
- The algorithm keeps track of two subsets of columns: a subset of columns currently accepted in the model and a subset of columns in the reference matrix that have not yet been considered.
- In each iteration of the algorithm, the column of the reference matrix that is best correlated with the regression error obtained in the previous iteration is added to the model and LMS parameter estimation is performed.
- An objective cost function is calculated from the determination coefficient $R^2$ and the complexity of the model as in Equation (9).
- If a considerable improvement of the objective function is found, a new iteration is considered with the current model, otherwise we return to the previous model and another column is tried.
- The algorithm stops once there are no further columns to try (the space of regressors has been explored).

## 4 Adaptive logical control

The control of the CUC can be done either concurrently with the system normal operation, or during idle times using the same test sequence considered in the design phase (in this last case, the Gaussian-like persistently exciting input sequence will be generated by the controller, which can allow the extraction of a more precise behavioural model). As shown in Figure 3, the input/output sequences obtained via the embedded sensors are used by the controller to estimate the parameters of the CUC behavioural model from which the performances are predicted.

### 4.1 Recursive parameter identification

For online and offline estimation of the parameter vector $\Theta$ of the behavioural model, we use a recursive LMS algorithm that process data on the fly, thus saving memory resources, and which requires only additions and multiplications by a constant. The algorithm is initialized as

$$\Theta^{(0)} = 0,\ Q^{(0)} = \rho I, \tag{11}$$

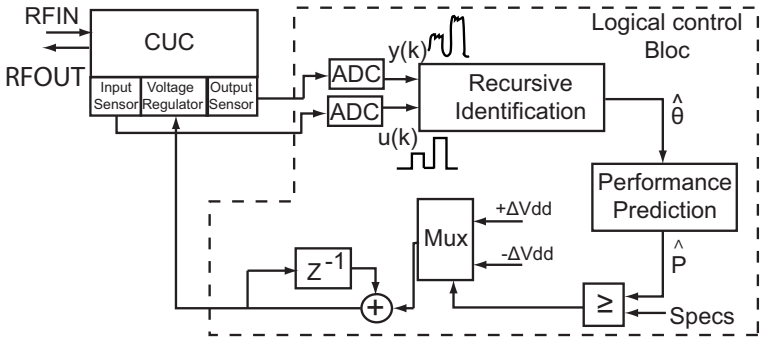



**Fig. 3.** Adaptive logical control strategy.

where $Q^{(0)}$ is an initial variance-covariance matrix formed by multiplying the identity matrix ($I$) by a positive constant $\rho$ (as discussed in Section 6). The classical recursive LMS algorithm is as follows

$$\begin{aligned} K^{(k)} &= \frac{\lambda^{-1}\ Q^{(k-1)}\ \gamma'(k)}{1+\lambda^{-1}\ \gamma'^{T}(k)\ Q^{(k-1)}\ \gamma'(k)}, 0 \ll\ \lambda\ \leq\ 1 \\ \varepsilon^{(k)} &= y^{(k)} - \gamma'^{T}(k)\ \hat{\Theta}^{(k-1)} \\ \hat{\Theta}^{(k)} &= \hat{\Theta}^{(k-1)} + K^{(k)}\ \varepsilon^{(k)} \\ Q^{(k)} &= \lambda^{-1}\ Q^{(k-1)} - \lambda^{-1}\ K^{(k)}\ \gamma'^{T}(k)\ Q^{(k-1)}, \end{aligned} \tag{12}$$

where $\gamma'^{T}(k)$ is a subset of the structure given by Equation (3), according to the selected model structure. The recursive parameter estimation stops once convergence is reached ($\varepsilon^{(k)}$ is smaller than a given constant) or a pre-defined number of iterations is attained.

### 4.2 Logical control strategy

The logical control is not intended to be permanently on. It is activated when the application sets a new performance mode for the CUC which requires a different CUC power supply. The control follows an iterative algorithm that starts with the CUC power supply set at the maximum value. During each iteration, the behavioural parameters $\hat{\Theta}$ are estimated by the LMS recursive algorithm and used by the regression equations to predict the CUC performances $\hat{P}$. These are in turn compared with the specifications required by the new performance mode. If the specifications are met, the power supply of the CUC is reduced by a pre-defined value $\Delta Vdd$ and a new iteration is considered. Otherwise, if the specifications are not met, the power supply is incremented by a value $\Delta Vdd$ and the control stops.

# 5 Case Study

## 5.1 LNA : Low Noise amplifier

Our CUC case-study is a Low Noise Amplifier (LNA) used in the 802.11g standard receivers that work in the 2.4 GHz ISM BAND. The LNA topology is presented in Fig. 4. This inductive degenerated cascade structure is compatible with narrow band applications and offers WiFi performances. The biasing stage of the circuit is formed by resistors R1, R2 and transistor M3. With the use of gate and source inductances, a real part of the input impedance can be generated without the need of actual resistances. Thus, inductors Lg and Ls provide appropriate input matching at 50 $\Omega$. Using this topology we can match the circuit without adding noise which implies a lower noise figure of the LNA. The gain stage is composed by M1 and M2. M1 provides the high gain, whereas M2 isolates the input from the output, reducing the Miller capacitor and eliminating the dependency between the gate-drain capacitance and the drain inductance. Increasing the reverse isolation is important for: (1) lowering the effect of the Local oscillator leakage produced by the following mixer, and (2) minimizing the feedback from the output to the input. At the output of the circuit, the parallel Ld-Cd tank resonates at 2.4GHz and the resistor Rd controls the gain at this frequency. The LNA is designed using the 0.25 um BiCMOS7RF technology provided by ST Microelectronics. The principle performances of the LNA at 2.4 GHz are: Gain>12 dB, NF <1.6 dB and IIP3 >5.9 dBm.

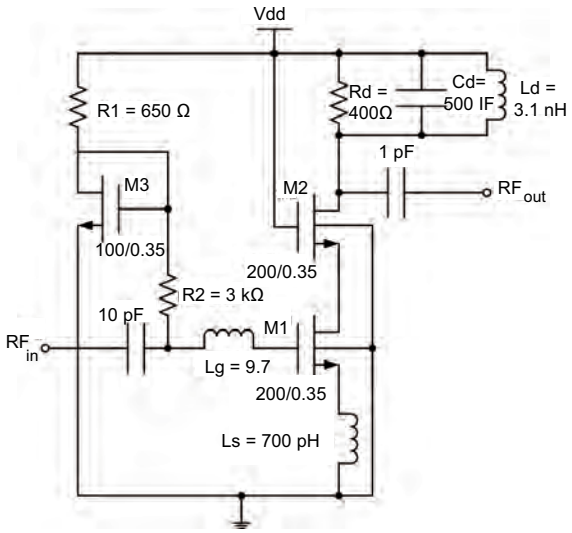



**Fig. 4.** LNA schematic.

### 5.2 Envelope Detector

Different sensors that extract RF power and convert it into a low-frequency signal for BIST purposes are available in the litterature [11][12][13]. We have developed an envelope detector, with a very simple architecture, based on the following design constraints: (a) minimum silicon area overhead, (b) high input impedance in the frequency range of interest to avoid undesired loading of the CUC, (c) high dynamic range suitable for testing different on-chip CUCs, and (d) wide band of operation to monitor CUCs that work at different frequencies involved in the system. This circuit consists of two stages as shown in Fig.5.

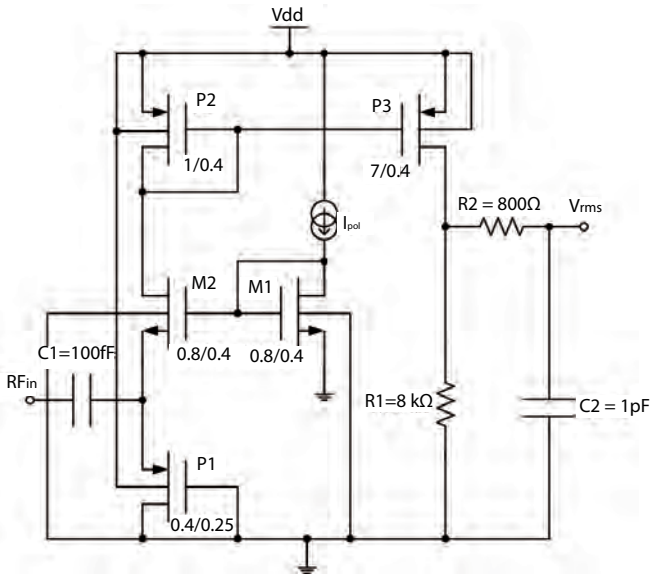



**Fig. 5.** CMOS envelope detector.

The first stage is a rectifier that performs half-wave rectification on the current delivered at the source of the transistor M2. The half-wave rectifier works as follows. The operating point of the transistor M2 is controlled by the bias current Ipol which flows through the diode-connected transistor M1. The difference between the fixed gate voltage of M2 and its source voltage is very close to its threshold voltage, such that M2 is at the verge of conduction. When the current passing thought the source of M2 is positive, transistor M2 is off and the current passes entirely through transistor P1 to the ground. During the negative half-cycle, the source voltage of M2 decreases which activates M2. During this half-cycle, the current flowing through M2 is copied and amplified through the current mirror formed by transistors P2 and P3. It is important to note that the sensitivity of the detector is mainly controlled by Ipol. In particular, as this current is reduced, the rectifier is sensitive to smaller signal amplitudes

and this characteristic is critical in an on-line monitoring scenario when the envelope detector is related to the input of the LNA. On the other hand, a main challenge exists between the high dynamic range of the envelope detector and its sensitivity. In the second stage, the amplified current is converted to voltage through Rout which is equivalent to the output resistor rds of the transistor P3 in parallel with the resistor R1. Finally, in the low pass filter R2-C2 a compromise exists between the time constant of the settling response and the ripple in the output voltage. The envelope detector has the following characteristics: an input impedance equal 1.5-11 kOhms in the band of operation 500 MHz -10 GHz, an input dynamic range of 35 dB and an area equal to 2170 $\mu m^2$, which corresponds to 0.543 % of the area of the LNA. Figure 6 plots the input-output characteristic of the envelope detector for the two edges of the frequency band. Furthermore, the study of the impact of the envelope detector on the LNA specifications is achieved by simulating the LNA performances with and without the envelope detector. The analysis shows just a low degradation thanks to the high impedance at the input of the envelope detector.

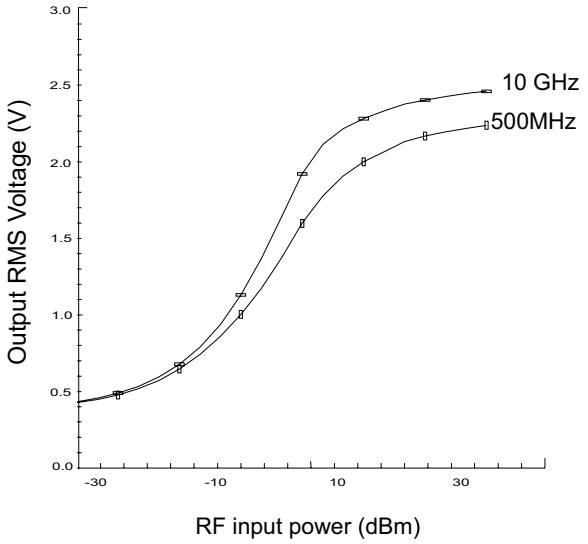



**Fig. 6.** Input-output characteristic of the envelope detector.

### 5.3 Variation of performances with the power supply voltage

**Input matching and input reflection parameter (S11).** The input reflection parameter reflects the matching at the input of the LNA. This parameter is principally influenced by the input impedance. As the input impedance of the

LNA gets closer to 50 $\Omega$, S11 becomes more negative. From the small signal model shown in Figure 7, the input impedance of the LNA is calculated as

$$-Vin + \frac{Iin}{sCin} + \frac{Iin}{sCgs} + sLg\ Iin + sLs\ (Iin + gm_1\ Vgs) = 0 \tag{13}$$

with s=jw, Cin is the input capacitor, Cgs is the gate to source voltage, Lg and Ls are respectively the gate and the source inductance and $gm_1$ is the transconductance of transistor M1 (notice that the transconductance of the overall cascode topology is equivalent to the transconductance of transistor M1).

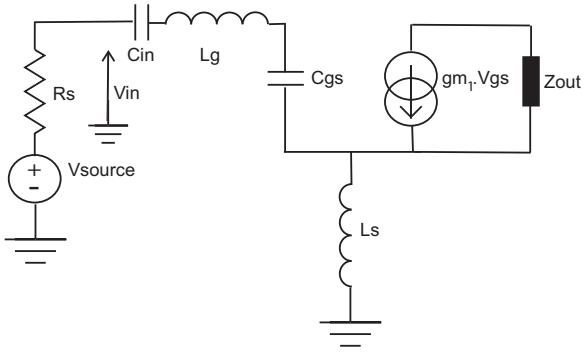



**Fig. 7.** Small signal model of the LNA

Since

$$Vgs = \frac{Iin}{sCgs} \tag{14}$$

Equation (13) can be written as

$$-Vin + Iin(\frac{1}{sCin} + \frac{1}{sCgs} + sLg + sLs + \frac{gm_1\ Ls}{sCgs}) = 0. \tag{15}$$

Since Cgs is very small compared to Cin

$$\frac{1}{sCin} + \frac{1}{sCgs} \approx \frac{1}{sCgs}, \tag{16}$$

the input impedance of the circuit is approximately given by

$$Zin \approx \frac{Vin}{Iin} = \frac{gm_1\ Ls}{Cgs} + s(Ls + Lg) + \frac{1}{sCgs}. \tag{17}$$

In order to accomplish the impedance-matched conditions at $w_0$ (equal to 2.4 GHz in our case), the LNA is designed such that the following condition is satisfied

$$w_0(Ls + Lg) = \frac{1}{w_0 Cgs}. \tag{18}$$

Thus, at 2.4 GHz the input impedance becomes

$$Zin = \frac{gm_1\ Ls}{Cgs} \tag{19}$$

which is the real part that should be equal to $50\Omega$. From Equation (19) we can deduce that Zin is proportional to the transcanductance $gm_1$ as given by

$$gm_1 = 2\ Kn\ \frac{W}{L}\ (Vgs - Vt). \tag{20}$$

The term Kn W/L is technology dependent. Vgs is controlled by the biasing stage of the circuit which is proportional to the power supply voltage, therefore $gm_1$ is directly proportional to the power supply voltage. At 3.3V the LNA is designed to be matched at $50\Omega$. Once the power supply voltage decreases, the input impedance will decrease and it will be far away from its initial value $50\Omega$ which degrades the input reflection parameter S11, then S11 increases.

**Gain (S21).** The LNA is the first gain stage in a receiver system. It must amplify the very low amplitude signal from the antenna adding a minimum amount of noise. The gain of the LNA is of critical importance. We will derive next the relation between the power supply voltage and the gain. The small signal analysis shows that

$$Vout = -Zout\ gm_1\ Vgs = -Zout\ gm_1\ \frac{Iin}{sCgs} \tag{21}$$

with

$$Zout = Cd//Ld//Rd//rds \tag{22}$$

rds is the output impedance of the cascode stage given by

$$rds = rds_1.rds_2.gm_2 \tag{23}$$

where $rds_1$ is the output impedance of the transisor M1, $rds_2$ is the output impedance of the transistor M2 and $gm_2$ is the transconductance of transistor M2. From Equations (17) and (21)

$$Vout = \frac{-Zout\ gm_1\ \frac{1}{sCgs}\ Vin}{Zin}. \tag{24}$$

Also, from Figure 7 we can deduce that

$$-V_{source} + Rs.Iin + V_{in} = 0 \tag{25}$$

and

$$V_{in} = \frac{V_{source}\ Zin}{Rs + Zin}. \tag{26}$$

From Equations (24) and (26)

$$V_{out} = \frac{-Zout\ gm_1\ \frac{1}{sCgs}\ Zin\ V_{source}}{(Rs + Zin)\ Zin} \tag{27}$$

and the gain of the LNA becomes

$$Gain = \frac{Vout}{Vin} = \frac{-Zout\ gm_1\ \frac{1}{sCgs}}{Rs + \frac{gm_1\ Ls}{Cgs} + s(Ls + Lg) + \frac{1}{sCgs}}. \tag{28}$$

At the resonant frequency and under impedance-matched conditions

$$w_0(Ls + Lg) = \frac{1}{sCgs} \tag{29}$$

$$\frac{gm_1\ Ls}{Cgs} = Rs. \tag{30}$$

Finally, by substitution in Equation (28) we obtain

$$Gain = \frac{Vout}{Vin} = \frac{-Zout\ gm_1\ W_0\ (Lg + Ls)}{2\ Rs}. \tag{31}$$

Hence we can see that the gain of the LNA is proportional to the tranconductance $gm_1$, which in turn is directly proportional to the power supply voltage. Thus, as the power supply voltage increases, the gain increases.

**Noise Figure (NF).** According to the Friis equation in a chain of n stages, the overall noise factor of the chain is expressed as

$$Ftotal = F1 + (\frac{F2 - 1}{G1}) + (\frac{F3 - 1}{G1G2}) + ... + (\frac{Fn - 1}{G1G2....Gn}). \tag{32}$$

This formula allows us to highlight the importance of the noise factor (F1) and the gain (G1) of the first block of a chain. It mainly determines the entire system noise. In order to define the dependence between the noise figure and the power supply voltage, we consider the noise model shown in Figure 8. We will use this model to calculate the ratio of the total noise power at the output to the noise power at the output due only to the input source. This ratio represents the noise factor [14].

Neglecting the 1/f noise and the gate noise, the input noise will be generated by the source resistor

$$V_{nRs}^2(f) = 4.k.T.Rs \tag{33}$$

with k the Boltzman constant, and T the absolute temperature. So the output noise power due to the input noise is given by

$$V_o^2 = V_{nRs}^2(f).\ Gain^2. \tag{34}$$

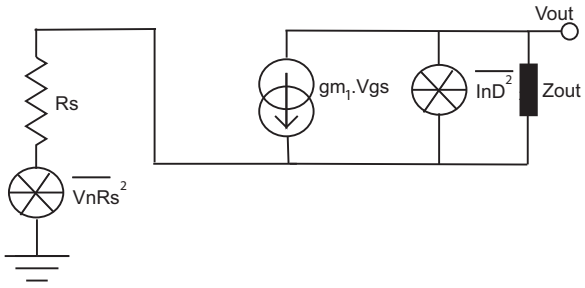



**Fig. 8.** Equivalent noise model ignoring gate noise

Additional output noise power comes from the thermal noise generated in the channel that can be expressed as

$$V_{nD}^2(f) = I_{nD}^2.Zout^2 \tag{35}$$

with

$$I_{nD}^2(f) = 4.k.T.\gamma.gm_1 \tag{36}$$

where $\gamma$ is a function of the transistor parameters and is approximated to 2/3 when considering the thermal noise in the channel without the substrate effect.

As a result the noise factor of the LNA in our case study is

$$F = \frac{V_{nD}^2(f) + V_{nRs}^2(f).\ Gain^2}{V_{nRs}^2(f).\ Gain^2} = 1 + \frac{V_{nD}^2}{V_{nRs}^2(f).\ Gain^2} \tag{37}$$

and using the previous expressions

$$F = 1 + \frac{4.\gamma.Rs}{gm_1.W_0^2(Lg + Ls)^2}. \tag{38}$$

Finally, the noise figure is given by

$$NF = 10\ log(F) = 10\ log(1 + \frac{4.\gamma.Rs}{gm_1.W_0^2(Lg + Ls)^2}). \tag{39}$$

This Equations shows that the noise figure is inversely proportional to $gm_1$. Thus, as the power supply increases, NF decreases.

**Non linearity effects (1dB compression).** We will derive next an expression for the 1dB compression point. Let $Vin(t)$ be the input signal of a system and $Vout(t)$ its output.The system behaviour can be modelled by

$$Vout(t) = \alpha_0 + \alpha_1\ Vin(t)\ +\ \alpha_2\ Vin^2(t)\ +\ \alpha_3\ Vin^3(t)\ + .... \tag{40}$$

For simplicity, we limit our study to the third harmonic. Considering an input signal Vin= Ain Cos ($w_0 t$) and developing Equation 40, we see that the output

amplitude of the signal at the fundamental frequency is a non linear function of the input amplitude

$$Aout = \alpha_1\ Ain\ + \frac{3\ \alpha_3\ Ain^3}{4} \tag{41}$$

where $\alpha_1$ is the linear gain of the amplifier. Thus in order to calculate the 1-dB compression, we should calculate the input amplitude $A_{1dB}$ for which the linear gain decreases of 1dB. For this, the gain equation (41) must be equal to the linear gain decrease of 1dB

$$20\ log(Gv) + \frac{3\ \alpha_3\ A_{1dB}^2}{4} = 20\ log\ Gv - 1dB. \tag{42}$$

Therefore the 1dB compression point is

$$A_{1dB} = \sqrt{0.145\ \frac{Gv}{\alpha_3}}. \tag{43}$$

In order to show the dependence between the $A_{1dB}$ and the power supply voltage, we assume the small input signal $Vin(t)$ around the bias (Vgs-Vt) so the output DC voltage is

$$Vout = Zout\ I_D = Zout\ \frac{Kn}{2}(Vgs - Vt)^2. \tag{44}$$

For a submicron technology, the channel length is of the same order of magnitude as the depletion-layer widths (xdD, xdS) of the source and drain junctions. Thus, taking into account the short channel effects, the drain current is assumed to be equal to

$$I_D = \frac{Kn(Vgs - Vt)^2}{2[1 + \theta(Vgs - Vt)]}. \tag{45}$$

Kn is a parameter dependent of the technology and $\theta$ is a factor that represents the velocity saturation and the mobility degradation. For an input small signal $Vin(t)$ around the bias voltage of the gate of the MOS (Vgs-Vt), the output Vout becomes

$$Vout = Zout\ I_D(t) = Zout\ \frac{Kn[Vin(t) + (Vgs - Vt)]^2}{2(1 + \theta[Vin(t) + (Vgs - Vt)])}. \tag{46}$$

Since $\theta$ is very small comparing to 1,

$$\frac{1}{1 + \theta[Vin(t) + (Vgs - Vt)]} \approx 1 - \frac{\theta[Vin(t) + (Vgs - Vt)]}{2} \tag{47}$$

and Equation (46) becomes

$$Vout = K[Vin(t) + (Vgs - Vt)]^2(1 - \frac{\theta[Vin(t) + (Vgs - Vt)]}{2}). \tag{48}$$

with K = Kn Zout/2. Developing this Equation

$$Vout = K(Vg - Vt)^2 - \frac{K\theta}{2}(Vgs - Vt)^3 + [2K(Vgs - Vt) - \frac{3K\Theta}{2}(Vgs - Vt)^2]Vin(t) + [K - \frac{3K\theta(Vgs - Vt)}{2}]Vin^2(t) - \frac{K\theta}{2}Vin^3(t) \quad (49)$$

and by comparison to Equation (43), we deduce

$$\alpha_1 = 2K(Vgs - Vt) - \frac{3K\theta}{2}(Vgs - Vt)^2, \quad (50)$$

$$\alpha_3 = -\frac{K\theta}{2}. \quad (51)$$

Thus the 1dB compression is equal to

$$A_{IP1} = \sqrt{0.145\frac{2K(Vgs - Vt) - \frac{3K\theta}{2}(Vgs - Vt)^2}{\frac{K\theta}{2}}}. \quad (52)$$

Considering now that $\theta$ is very small compared to 1 (then $3(Vgs - Vt)^2$ can be ignored), (52) becomes

$$A_{IP1} = \sqrt{0.145\frac{4K(Vgs - Vt)}{\theta}}. \quad (53)$$

This Equation shows that $A_{IP1}$ is proportional to the gate bias voltage (Vgs), therefore, when the power supply voltage decreases, $A_{IP1}$ decreases.

**Non linearity effects (IIP3).** We will see next the effect of the power supply on the third order interception point. Considering Equation 40 for an input signal Vin = A cos($w_1$t) + A cos($w_2$t), we obtain

$$Vout = [\alpha_1 + \frac{9\alpha_3 A^2}{4}]Acos(w1(t)) + ... + \frac{3}{4}\alpha_3 A^3 cos(2w1 - w2) + \frac{3}{4}\alpha_3 A^3 cos(2w2 - w1). \quad (54)$$

Since $\alpha_1$ is very large compared to $\frac{9\alpha_3 A^2}{4}$ [14], the input level for which the output components at w1 and w2 have the same amplitude as those at 2w1-w2 and 2w2-w1 is given by

$$\alpha_1 A_{IP3} = \frac{3\alpha_3 A^3}{4}. \quad (55)$$

Thus the input IP3 is:

$$A_{IP3} = \sqrt{\frac{4}{3}\frac{Gv}{\alpha_3}}. \quad (56)$$

Using now a similar development as for Equation 43 we obtain

$$A_{IP3} = \sqrt{\frac{16(Vgs - Vt)}{3\Theta}}. \tag{57}$$

As in the case of 1dB compression point, Equation (57) shows the proportionality between the power supply voltage and the third input intercept point.

**Isolation parameter (S12).** As we mentioned above, the transistor M2 increases the isolation between the input and the output and as the isolation increases, S12 decreases. In this section we will show the dependency between the isolation and the power supply voltage. Using the Miller theory, the input-output impedance can be expressed as

$$Z = Z_{Miller}[1 - G(f)] \tag{58}$$

where Z is the impedance between the input and the output and G(f) is the gain at the defined frequency. At the resonant frequency the term 1-G(f) increases as the power supply increases. This increases the input-output impedance, improving the isolation, so S12 decreases.

**Isolation parameter (S22).** S22 is the output port voltage reflection coefficient. The value of S22 decreases as the adaptation of output impedance approaches to 50 $\Omega$. The output LNA impedance of the LNA is calculated by supposing a fictitious source voltage $V_{fict}$ at the output that generated a fictitious current $I_{fict}$ and then we calculate the output impedance as the ratio between $V_{fict}$ and $I_{fict}$. Notice that when we calculate the output impedance, the input source voltage should be grounded and the current source should be opened in the small circuit analysis thus

$$Zout = Ld//Cd//Rd//rds1.rds2.gm2. \tag{59}$$

Since Rd is very small compared to rds1.rds2.gm2, we can deduce that, at the resonant frequency, the output impedance of the proposed architecture is mainly controlled by Rd which is independent from the power supply voltage.

### 5.4 LNA performance modes

The above analysis has been verified by simulation for the case-study LNA. Figure 9 shows transient-level simulations of the performance variation when the power supply is varied, for all performances except S22 (which does not vary significantly). These variations are in all cases monotonic.

For a typical application, gain and noise figure are the most important LNA performances to be controlled. S11 and S12 typically have maximum values that cannot be exceeded (e.g. $S11 < -10dB$ and $S12 < -40dB$). Similarly, IIP1

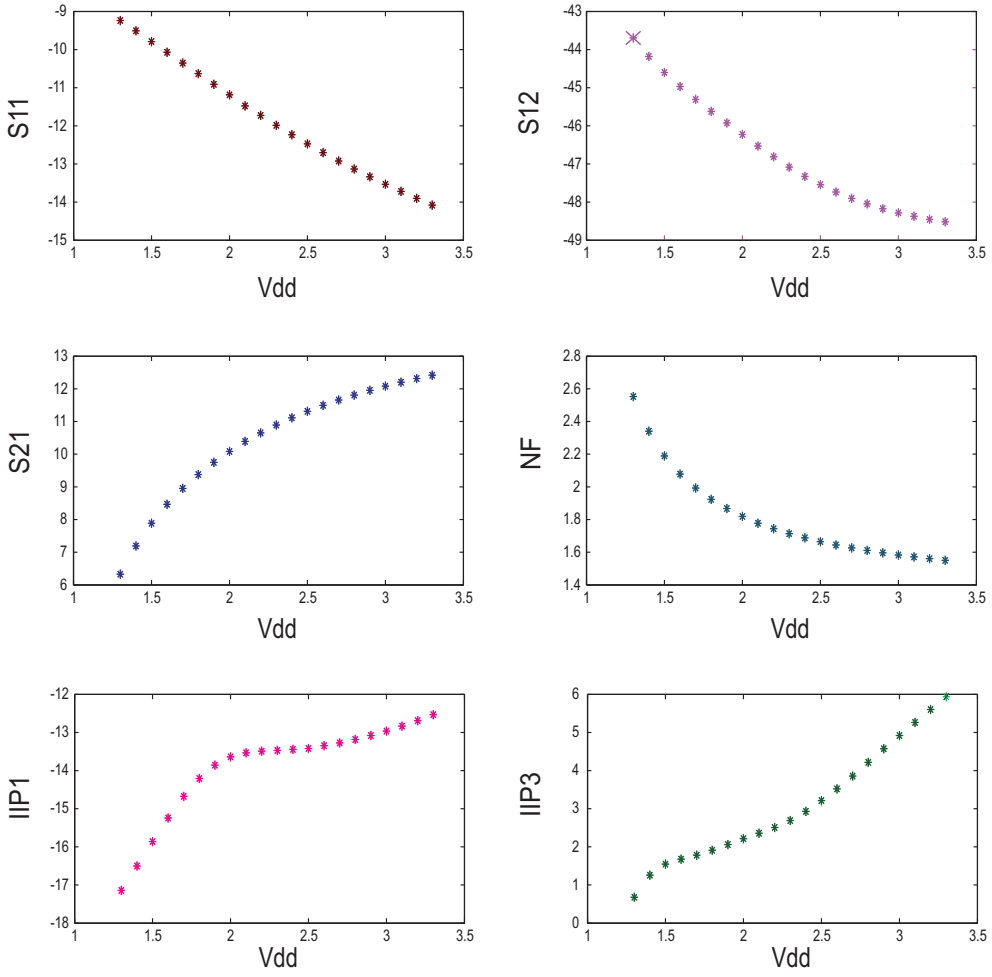



**Fig. 9.** LNA performances versus power supply.

and IIP3 have minimum values that cannot be exceeded (e.g. $IIP1 > -20dBm$, $IIP3 > -10dBm$).

As an example, we define three different performances modes: a MAX mode of maximum power supply, a MIN mode of minimum power supply and an INT mode of intermediate power supply. In all modes, the above conditions for S11, S12, IIP1 and IIP3 must be respected. In MAX mode, $Gain > 11.5dB$ and $NF < 1.65dB$. In INT mode, $Gain > 10dB$ and $NF < 2dB$. Finally, in MIN mode, $Gain > 8dB$ and $NF < 2.2dB$.

The level of power supply required by each performance mode will be set by the controller. For later reference, Figure 10 shows the power consumption of the CUC as a function of the power supply voltage obtained by transistor-level simulation.

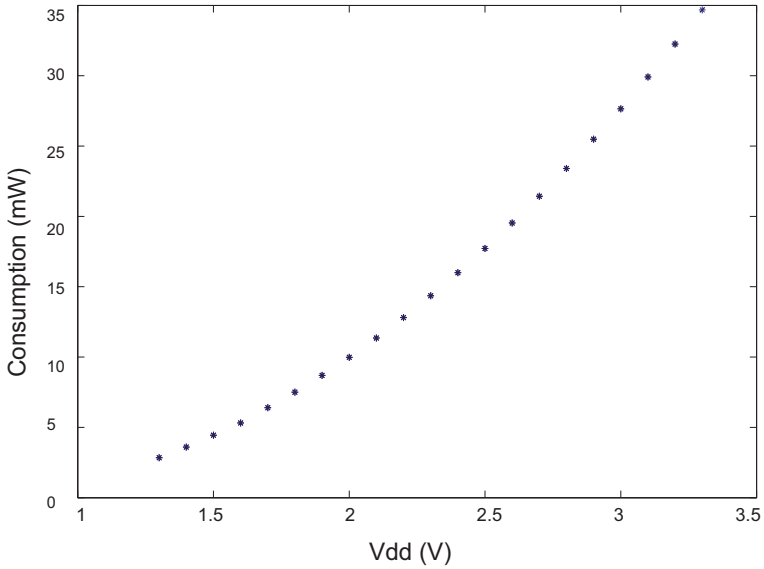



**Fig. 10.** LNA consumption versus power supply

## 6 Simulation results

For building the behavioural and predictive models for the CUC of Figure 4, the CUC input stimulus is obtained by mixing a Gaussian signal with an average amplitude of 150 mV, sampled at 10 MHz, with a carrier signal at 2.4 GHz. As shown in Figure 11, 200 values of u(k) and y(k) are obtained for a simulation time of 10 us (the mixer and the ADC/DAC converters are considered ideal).

A Monte Carlo transistor-level simulation of the CUC, with N =1000, has been performed for three different levels of power supply: 3.3 V (maximum power

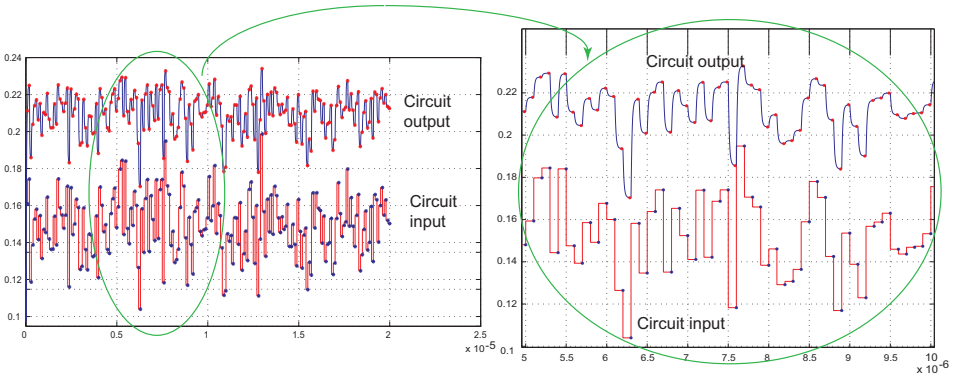



**Fig. 11.** Sampled input and ouput signal

supply voltage), 2.3 V and 1.3 V. For each level of power supply, the 200 values of the input/output sequences of each circuit sample are used by the algorithm of Figure 2 to identify the model structure. In the three cases, the following model structure has been retained:

$$y(k) = \theta^0 + \theta^1 u(k) + \theta^2 u(k)^2 + \theta^3 u(k)^3. \tag{60}$$

This behavioural model gives a determination coefficient $R^2$ higher than 98% for all 3000 circuit samples. For example, the model identified for the 5-th circuit sample is given by

$$y_5(k) = -0.03 + 0.78\ u(k) - 3.37\ u(k)^2 + 6.76\ u(k)^3. \tag{61}$$

Figure 12 compares the value predicted by the model and obtained by simulation of the circuit for 100 different time points. The predicted and the actual values are very close.

A prediction model is built using Branch and Bound algorithm for each performance. The prediction equations use only the parameters $\theta^0, \ldots, \theta^3$ of the behavioural model to predict the values of all CUC performances, as shown in Figure 13.

The simulation of the adaptive logical control strategy has been performed by considering the CUC at transistor-level and the controller modelled in Verilog A. The CUC is stimulated by the same stimulus described above. Initially, the CUC is set at the MAX mode, where the maximum power supply of 3.3 V is required. Next, we simulate the transition to a MIN mode, for which the performances are specified as indicated in Section 5.4.

Figure 14 shows the different iterations of the algorithm. Each iteration lasts 30 us, with the convergence time for the recursive parameter identification algorithm being somewhat smaller. This Figure also illustrates the convergence of the behavioural parameter $\theta^0$, for different iterations. The choice of values for the variables in the recursive LMS algorithm is important, in particular $\theta^0$, $\rho$

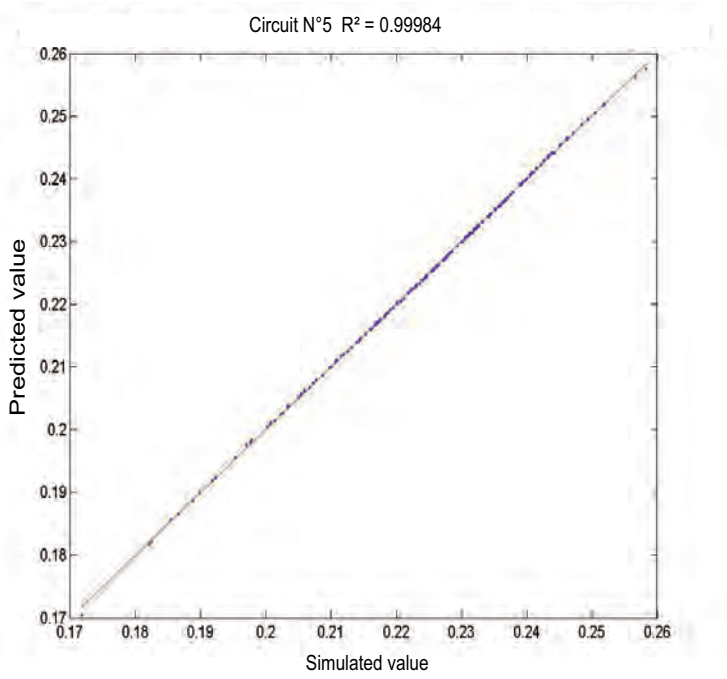
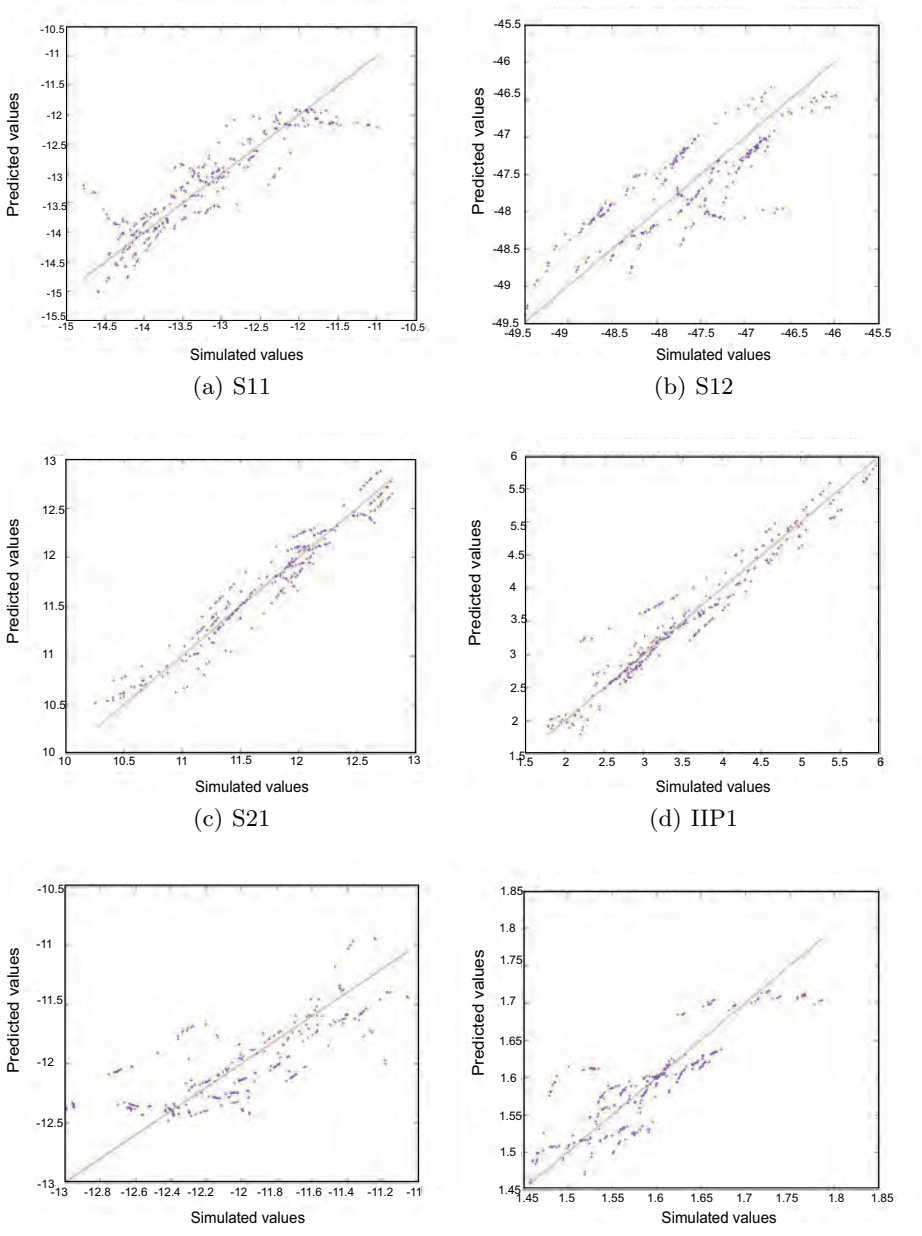



**Fig. 12.** Predicted and simulated output values of the CUC




(a) S11 (b) S12

(c) S21 (d) IIP1

(e) IIP3 (f) NF

**Fig. 13.** LNA performances prediction

and $\lambda$ in Equations (11) and (12). The value of $\rho$ must be as large as possible. The closer the value of $\lambda$ to 1 the slower the convergence of the algorithm, but the variance of $\hat{\theta}$ after convergence is smaller, oscillating around the optimum value. If $\lambda$ is closer to 0, the opposite behaviour is observed.

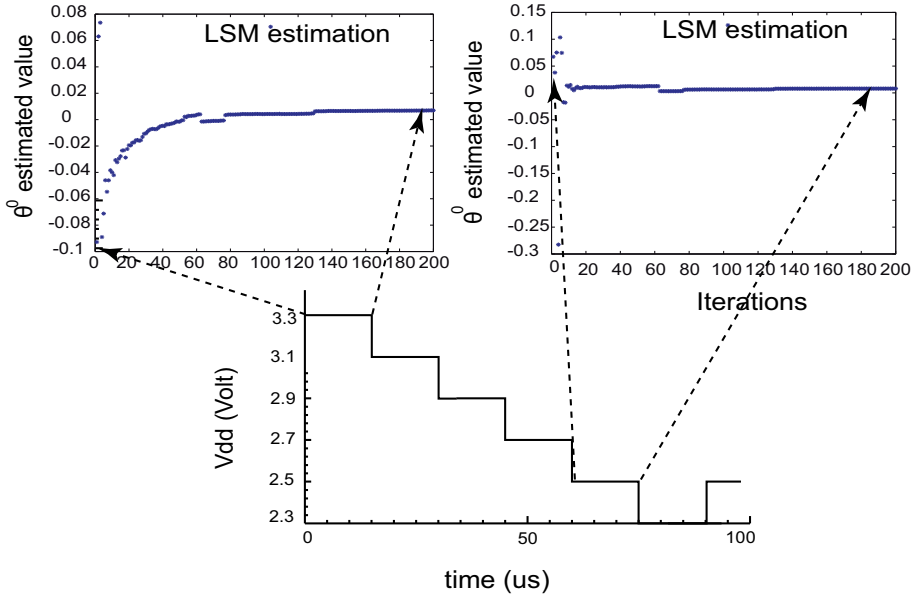



**Fig. 14.** Transistor-level simulation of the control strategy.

The circuit performances are estimated by the end of each iteration, once convergence has been achieved. Figure 14 shows that the control algorithm needs six iterations to reach a power supply voltage level of 2.3 V for which one of the specifications of the MIN mode is no longer respected. In the next iteration, the control stops with a power supply voltage level of 2.5 V, since the controller uses power supply voltage steps of 200 mV (this large value is used here to reduce simulation time). Table 1 illustrates the evolution of the performances predicted, and the reduction of power consumption at each level of power supply voltage (according to Figure 10). For example, the MIN mode with the power supply controlled at 2.5 V has a power consumption reduction of 54%.

## 7 Conclusion

This work has presented a new approach for reducing power consumption in RF devices based on adapting the power supply voltage by means of a logical control strategy. This strategy relies on embedded sensors, real-time parameter

**Table 1.** Performance prediction during logical control.

| Vdd (V) | Saved power(%) | Predicted/simulated values | NF $\leq 2.32$ | S11 $\leq -10$ | S12 $\leq -40$ | Gain $\geq 6.2$ | IIP1 $\geq -20$ | IIP3 $\geq -3$ |
|---|---|---|---|---|---|---|---|---|
| 3.1V | -14 | Prediction | 1.70 | -12.46 | -43.65 | 10.41 | -16.29 | 1.92 |
| | | Simulated value | 1.57 | -13.72 | -48.37 | 12.20 | -11.61 | 5.26 |
| 2.9V | -26 | Prediction | 1.74 | -12.30 | -43.23 | 10.06 | -17.09 | 1.06 |
| | | Simulated value | 1.59 | -13.33 | -48.17 | 11.95 | -11.83 | 4.57 |
| 2.7V | -38 | Prediction | 1.99 | -12.23 | -42.99 | 8.97 | -18.58 | 0.66 |
| | | Simulated value | 1.62 | -12.91 | -47.90 | 11.65 | -12.03 | 3.85 |
| 2.5V | -49 | Prediction | 2.25 | -11.96 | -42.88 | 7.86 | -19.70 | 0.39 |
| | | Simulated value | 1.66 | -12.47 | -47.54 | 11.31 | -12.19 | 3.21 |
| 2.3V | -54 | Prediction | 2.39 | -11.35 | -42.90 | 7.16 | -19.73 | 0.22 |
| | | Simulated value | 1.71 | -11.98 | -47.08 | 10.89 | -12.26 | 2.6902 |

identification and performance prediction, and makes use of simple on-chip resources. Significant power savings have been demonstrated at the transistor-level for an RF LNA with different performance modes. The control algorithm can guarantee the required specifications for each performance mode, despite circuit parametric deviations due to the manufacturing process or ageing mechanisms. Current work is aimed at validating this approach in hardware.

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