IMPACT OF GATE LEAKAGE ON EFFICIENCY OF CIRCUIT BLOCK SWITCH-OFF SCHEMES

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Abstract: Two different schemes to switch-off unused circuit blocks (ZigZag-cut-off scheme[1] and n-/p-block MTCMOS cut-off scheme[2,3,4,5,6] are examined in deep-submicron technologies by analytical investigation and simulation. The theoretical basis of the ZigZag-scheme is given and particular design constraints are discussed. It is shown that the power-saving benefits of the ZigZag-scheme are critically dependent on the gate-leakage, whereas n- or p-block switching keep their effectiveness. Finally it is derived that n-block switching tends to cause severe glitch activity during power-up process degrading both power-up-time and energy loss. The ZigZag-scheme however does not suffer from this effect. The advantages and drawbacks of the two schemes are compared depending on the available technology generation. Finally recent extensions to ZigZag are discussed.

Key words: MTCMOS, ZigZag, ZZSCCMOS, Circuit Block Switch-Off, Sleep-Transistor Scheme, Gate-Tunneling, GSCMOS

1. INTRODUCTION

Ongoing technology scaling increases speed and area efficency of digital systems, but transistor parasitics increase rapidly and effects up to now neglected gain strong influence on circuit and system design. Even in low-power devices off-currents increase by a factor of ten per technology node[7]. Consequently for SoC efficient power management strategies on transistor as well as on system level are required both in mobile and in high-end

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applications. Among others, a very promising concept is to turn-off unused circuit blocks by separating them from the supply (power-gating)[2,3,4,5,6].

Beside the task of finding the optimum switch dimension[8,9], there are a couple of possibilities to position the switch relatively to the logic[1,3]. A recently proposed strategy is the so called ZigZag-scheme that uses both an n-channel and a p-channel switch and assigns the different gates either to one switch or to the other one[1]. In this paper we describe the theoretical principles and technological suppositions of the ZigZag-scheme and derive the particular design rules for this scheme. Thereafter we discuss the different loss mechanisms for conventional power switching and ZigZag-scheme. The scaling of the different mechanisms is examined for state of the art deep-sub-micron technologies and extrapolated to future technologies.

Subsequently we discuss the behaviour of a circuit block during activation for conventional and ZigZag-schemes. Predictions about scaling limits and circuit behaviour are derived analytically and proven by simulation. This paper represents an example of technology dependent design: In deep sub-micron-CMOS not only transistor level but even system level design depends severely on technology properties. Therefore every technology generation will require its own adopted design strategy.

2. LEAKAGE-MECHANISMS IN DEEP-SUB-MICRON CMOS

At the beginning of the CMOS era standby power dissipation wasn't worth mentioning because of the high threshold voltage, long channels, thick gate oxides etc. During the last years reduction of the supply voltages required low threshold voltages in order to meet the performance requirements. The subthreshold current given by

$$I_S = I_0 \exp\left(\frac{V_{GS} - V_{th}}{\eta V_T}\right)\left(1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right); \qquad I_0 = \mu_{eff} C_{ox} V_T^2 (\eta - 1)\frac{W}{L} \qquad (1)$$

is exponentially dependent on the threshold voltage V_{th} and therefore becomes more and more important. Scenarios given by the ITRS-Roadmap[7] predict the subthreshold current, together with the gate-tunneling current covered next, to be the dominant mechanisms of power dissipation in future CMOS technologies. In a logic circuit with the effective gate width W_{eff}^{n} of all n-channel branches and W_{eff}^{p} of all p-channel branches, the average static power dissipation caused by subthreshold current can be estimated as:

$$P_{sub} = \frac{1}{2}\left(W^n_{eff} I'_n + W^p_{eff} I'_p\right) \cdot V_{DD}; \qquad I'_n = I'_{0n} exp\left(-\frac{V^n_{th}}{\eta V_T}\right) \quad I'_p = I'_{0p} exp\left(\frac{V^p_{th}}{\eta V_T}\right) \tag{2}$$

I_n' and I_p' describe the subthreshold currents of the n-channel and the p-channel transistors respectively normalized to the gate width. There are two characteristics of the subthreshold current that are important for this work: Although Eq. (1) indicates that for voltages $V_{DS} >> V_T$ the current is not a function of this voltage, the subthreshold current is exponentially dependent on V_{DS} because of the influence of Drain Induced Barrier Lowering (DIBL) on the threshold voltage in short channel devices:

$$V_{th} = V^0_{th} + V^1_{th} V_{DS}; \; V^1_{th} := \frac{d}{dV_{DS}} V_{th}\Big|_{V_{DS}=0} \tag{3}$$

The second property is the temperature dependence of the threshold voltage.

Another type of leakage which gains more and more importance, if gate oxide thickness is scaled further, is the leakage produced by the gate-tunneling current. In the general case it is very difficult to describe the flow of carriers over a tunneling barrier[10,11], but fortunately the tunneling in static CMOS logic is very simple, because apart from the switching process, there are only two states of transistor operation: Either the transistors are in linear region with a vanishing V_{DS} , or they are in subthreshold region. In the first case, there is a location-independent inversion channel. Thus the tunneling current is constant below the whole gate. The tunneling out of the source and drain overlap region respectively is different from the current density out of the channel, but because one single channel length is used the channel-to-overlap ratio is constant and the tunneling currents through the different transistor regions can be merged into an effective current density:

$$\begin{aligned} I_T &= \int_A j(x,y)\, dxdy \\ j_T &= \frac{\partial I_T}{\partial y} = \int j(x,y)\, dx \\ A: &\quad \text{Area under Gate} \\ j(x,y): &\quad \text{local density of tunneling current} \\ j_T: &\quad \text{tunneling current per unit width} \end{aligned} \tag{4}$$

In this context current density does not mean current per unit area but current per transistor width. The second important factor controlling the tunneling current is the potential drop across the gate oxide, which in static CMOS is given by the supply voltage V_{DD}-V_{SS}. For low voltages one effect of this potential drop is the impact on the shape of the potential barrier, but the more important one is the influence on the inversion charge density.

In the case of a transistor operating in subthreshold region, there is no inversion channel under the gate. The only leakage path is the drain-to-gate overlap region. Although there is a voltage drop of V_{DD}-V_{SS} across the barrier, the total current is smaller because of the reduced tunneling area.

3. CONVENTIONAL POWER-SWITCHING

With ongoing technology scaling, standby-power dissipation gets an important impact on the standby-time of mobile systems or the thermal power in high performance digital systems, respectively. Therefore different methods of switching-off unused circuits have been proposed. (MTCMOS = Multi Threshold CMOS combined with Circuit-Block-Switch-Off (CBSO)) Usually these schemes use one or more cut-off transistors that separate the unused logic block from the power-rails. Normally n-switches are preferable because of their lower on-resistance. The width of the switch transistors can usually be chosen much smaller than the total transistor width of the logic, therefore the total leakage is reduced. To reduce the leakage further, several techniques have been proposed in literature:

- high V_{th} switch-off-devices
- small switch width and boosting of switch device during active mode
- negative (positive) V_{GS} for switches in off-state (super-cut-off)[6]

If the leakage of the switch transistor is much lower than the total leakage of the logic, each node capacitance in the logic block will be charged (or discharged) by leakage to a potential near the unswitched power-rail. For instance switching-off a logic block by an n-channel device between V_{SS} and the circuit and waiting for a short time, each signal node and even the switched power-rail, which is referred to as virtual power-rail (V_{VSS}), reach the same potential slightly below V_{DD}. As a result all transistors operate in subthreshold region.

The upper bound of the remaining leakage current is determined by the subthreshold and gate-tunneling current of the switch device. For thick-oxide-switches the gate-tunneling current is negligible and the standby-power dissipation is given by

$$P_{standby}^{CBSO} = I'_{0S}\, exp\left(-\frac{V_{th}^{switch}}{\eta V_T}\right) W_{switch} \cdot V_{DD} \tag{5}$$

To describe the gain in standby power dissipation we introduce the leakage-reduction-ratio (LRR), which is the ratio between the total leakage in active and in inactive mode:

$$\begin{aligned} LRR &= \frac{\frac{1}{2}\left(W^{n}_{eff} I'_{n} + W^{p}_{eff} I'_{p}\right) + I^{logic}_{gate}}{I'_{S} W_{switch}} \\ I'_{S} &= I'_{0S}\, exp\left(-\frac{V^{switch}_{th}}{\eta V_{T}}\right) \end{aligned} \tag{6}$$

It is important to notice that there is no significant gate-tunneling current in a cut-off logic block because a few moments after switching-off the circuit, each node within the block has the same potential.

Summarizing: All schemes cutting-off the V_{DD} or V_{SS} power-rail (n-block or p-block-switching respectively) reduce the standby power significantly and suppress additional gate leakage paths completely. Therefore these schemes can be called gate-leakage tolerant strategies and will therefore also be applicable in future technologies with significantly higher gate leakage.

4. PRINCIPLE OF ZIGZAG-SCHEME

The main disadvantage of n- and p-block switching respectively is that all nodes are charged or rather discharged after switching-off the circuit. After turning on the system again, approximately half of the nodes have to be discharged to a logical zero and the rest of the nodes have to be recharged to a logical high state. This process requires not only energy, but also a significant power-on-time which contributes directly to the minimum power-down time, i.e. the minimum period of time for which it is useful to suspend a block by cutting-off the power supply. However, to minimize total leakage losses the power-on time should be as short as possible. The idea finally leading to the ZigZag-scheme[1], is to reduce the voltage swing of the virtual power rail, to maintain the system state at each logical node and not to increase total leakage over the switch. All this is possible by using both n-block and p-block switches and assigning each gate to one of these switches in a sophisticated way.

Assume a one-stage static CMOS gate with a particular logic level at its output. If this gate is assigned to the switch that cuts-off the power rail complementary to the output level, the logic level of the circuit will be conserved and the output capacitance does not have to be recharged. Furthermore the transistors, which operate in subthreshold region, are subject to the stack effect as they are in series with the switch transistor, i.e.

they get a negative V_{GS} and a reduced V_{DS} compared to the active-mode. In contrast to n- or p-block switching, even in off-state there is a non-vanishing V_{DS} voltage of the transistors in the switched block. Thus the voltage swing of the virtual power-rails is reduced. The strategy of assigning each gate to the proper cut-off switch can be verbalized as follows:

1. Assure fixed valid logic levels at all inputs during the power-down phase
2. Calculate the level of each node as if the circuit was not switched-off
3. Analyze each gate: If the output is high, assign the corresponding gate to the n-switch. If the output is low assign the gate to the p-switch.

The benefits of the ZigZag-Scheme depend on the strong monotonicity of subthreshold current around V_{GS}:

$$\left.\frac{\partial I_D}{\partial V_{gs}}\right|_V > 0 \quad \text{for each} \quad V \in K_\epsilon(0) \tag{7}$$

5. INPUT CIRCUITRY FOR ZIGZAG-SCHEME

The theory of the ZigZag-Scheme states that the cut-off switch should be in series to the non-conducting transistor group (n-block or complementary p-block). Indeed this includes that complex gates are allowed, but only those that have a single stage structure. Multi-stage gates would require that the first stage is assigned to one and the following stage to the other switch. This is not practical for library based design flows.

The main difficulty is that for the switch assignment the logical state has to be known for the whole block, especially for the input vector. Thus in most cases it will be necessary to set this condition explicitely before the system can be switched off. Unfortunately this state-forcing procedure requires additional energy and therefore the minimum power-down time increases. We propose four different methods to assure the system state:

1. Driving each input with a resetable flipflop the output stage of which is not switched-off[1].
2. Input multiplexers: Inserting additional gates (NAND or NOR gates for instance) that in dependence of a control signal at the first input transmit either the second input or a fixed level to the output. This method means some area overhead and a slightly longer critical path. Another drawback

is the high fan-out control signal that has to be valid during power-down period.

3. Special Input gates: These gates disconnect the input and assure the required logic level by an additional state-keeper transistor. Slight area and delay penalties result from this method.
4. Additional power rails: The idea of this method is to use additional power rails for the first logic stage. The gates of this stage do not operate in ZigZag-mode. By selecting a n- or p-switch their output level can be ensured without knowledge of the input vector. Anyway, this level does not correspond exactly to any supply potential as the output node is floating. Because of timing reasons this strategy means a serious area overhead.

It should be mentioned that the inner state of a circuit block before cut-off has to be known during design. Hence ZigZag scheme cannot be applied if the inner state has to be conserved by state retention flip-flops. Special state retention flip-flops forcing a certain output level during sleep mode and switching to the conserved level after activation can be used but result in additional switching activity. The additional energy overhead of this switching process increases the minimum sleep time.

6. POWER CONSUMPTION IN ZIGZAG-CBSO

As mentioned above, in a purely n-block or p-block switched system, respectively, the residual leakage is given by the properties of the switch transistor only:

$$I_{standby}^{n-CBSO} = W_s I_s' \tag{8}$$

In a ZigZag environment all logic nodes retain their respective logic levels, and therefore about half of all transistors operate in triode region, where there is a channel under the total gate area. The potential drop over their gate oxides is equal to the supply voltage V_{DD}-V_{SS}. Thus, conditions for maximum gate-leakage currents are given, according to section 2.

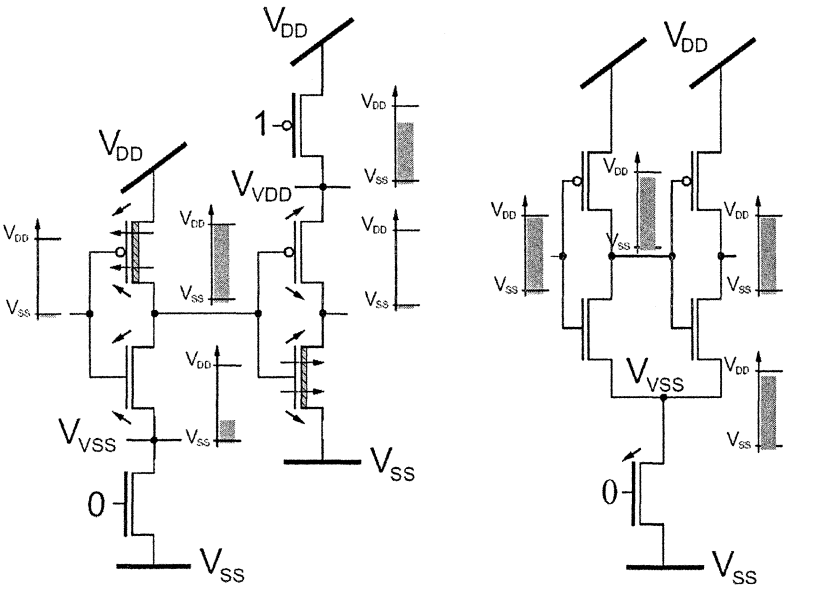

Figure 1. Principle of ZigZag-scheme (left) and n-block sleep transistor scheme (right) with node potentials and gate-tunneling paths.

The different tunneling paths are depicted in Figure 1. Consequently, in a ZigZag-environment the non-vanishing gate currents represent an additional leakage mechanism and in spite of the stack effect one has to expect an increased total leakage compared to an n- or p-block switching scheme:

$$\begin{aligned} I_{standby}^{ZigZag} &= W_S I'_{Sn} r + \frac{1}{2}\alpha \left(j_T^n W_{eff}^n + j_T^p W_{eff}^p \right) \\ r &:= \omega r_n + (1-\omega)\frac{I'_{Sp}}{I'_{Sn}} r_p \\ r_n &:= exp\left(\frac{V_{th,Sn}^1}{\eta V_T} (V_{DD} - V_{VSS}) \right) \\ r_p &:= exp\left(-\frac{V_{th,Sp}^1}{\eta V_T} V_{VDD} \right) \end{aligned} \tag{9}$$

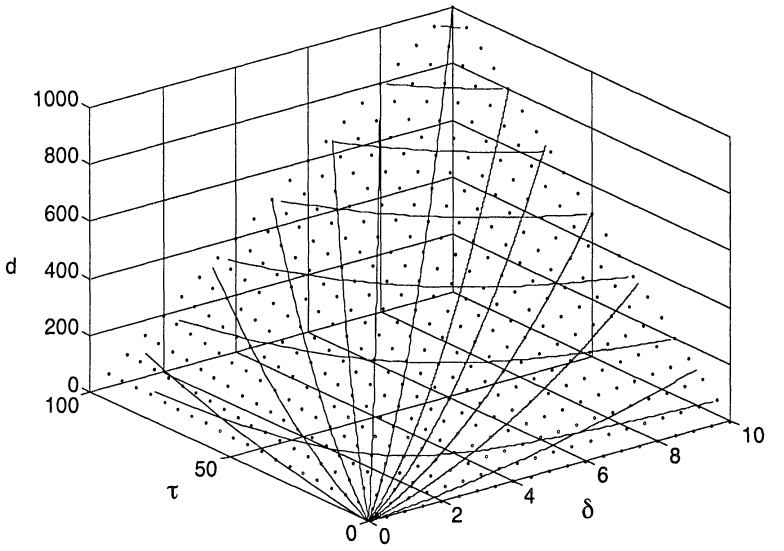

Figure 2. Dependence of degradation factor d on the design parameter δ and the technology parameter τ.

r is a correction because of the usage of two different types of switch transistors with width ratio

$$\frac{W_s^n}{W_s^p} =: \frac{\omega}{1-\omega} \tag{10}$$

and r_n and r_p respectively describe the reduced subthreshold current of the switches caused by the reduced swing of the virtual power-rails. α is an empirical factor describing the fact that the tunneling current is determined not by the effective gate width but by the total gate area of the active transistors.

The relative difference between the two schemes is given by

$$\begin{aligned} d &:= \frac{\Delta I_{standby}}{I_{standby}^{n-CBSO}} \\ &= r - 1 + \frac{\alpha}{2W_s I_s'} \left(j_T^n W_{eff}^n - j_T^p W_{eff}^p \right) \end{aligned} \tag{11}$$

Using the approximation $W_{eff} := W_{eff}^{n} = W_{eff}^{p}$ and substituting $j_T := \frac{1}{2}\left(j_T^n - j_T^p\right)$:

$$d = r - 1 + \frac{\alpha j_T}{I_s'}\frac{W_{eff}}{W_s} =: r - 1 + \tau\delta \tag{12}$$

The surface of the degradation factor d of the ZigZag-scheme is defined by the technology dependent quantity $\tau := \frac{\alpha j_T}{I_s'}$ and the design dependent quantity $\delta = \frac{W_{eff}}{W_s}$. The constant $g := r - 1$ describes the structural gain of the ZigZag-scheme (mostly negligible), i.e. the reduced subthreshold current of the switch devices caused by the smaller swing of the virtual power rails.

Equation 12 is plotted in Figure 2. It states that for large effective logic widths W_{eff} compared to the switch transistor widths and/or large tunneling currents in the total logic compared to the leakage of the switch, the ZigZag-scheme looses more and more its leakage suppression capability. The first condition is mostly valid in circuits with a large logic depth and many complex gates. The latter assumption is prone to occur in sub 100 nm high-performance technologies: In order to supress leakage effectively, the switch normally is made up of a high-V_{th}, thick oxide and/or super-cut-off[6] device. The logic however consists of leaky low or ultra-low-V_{th} devices with thin oxides. The following table shows a scenario for τ depending on transistor parameters specified by the ITRS-Roadmap:

Table 1. Efficiency of ZigZag scheme in future technologies predicted by ITRS-Roadmap

YEAR	2001	2002	2003	2004	2005	2006
L [nm]	90	75	65	53	45	40
I_S' @ 25C [pA/µm]	1	1	1	1	1	1
EOT [nm]	1.45	1.35	1.3	1.15	1.05	0.95
j_T [10^3 pA/µm]	4.64	14.4	25.6	144	464	1200
$\tau/\alpha = j_T / I_S'$ [10^3]	4.64	14.4	25.6	144	464	1200

7. POWER-ON PROCESS

The behaviour of the ZigZag-scheme during the power-on process differs significantly from the n- or p-block switching. As mentioned above in an n-block switching scheme each node is charged to a high potential. If the cut-off switch turns on, the V_{VSS} potential will break down quickly. Therefore both the gate-to-source and the drain-to-source voltages of all n-channel devices increase, subthreshold current increases exponentially and all logic nodes start discharging. Consequently the corresponding voltages of the p-channel-devices decrease causing an increased short-circuit current. When

the V_{VSS} potential drops further the gate-to-source voltages of some n-devices reach the threshold voltage and the node capacitances connected to the corresponding gates discharge even faster. If their voltage is low enough the n-devices of the following stage turn off and these stages charge their outputs to V_{DD}. Although this process means additional energy loss, the main problem is the following: At the beginning each node and each gate have the same state. The size of the different capacitances as well as the drivability of the connected gates determine how fast the different nodes are discharged and therefore whether a particular node is discharged completely or recharged. However the final state is determined by the input vector and the logical topology of the circuit. Consequently there exists a significant glitch probability because of the two competing mechanisms described above. These glitches cause additional dynamic losses and enlarge the power-on time significantly. Both phenomena increase the minimum power-down time and debase the applicability of the scheme.

In the ZigZag-scheme however, each logic node keeps a valid level compatible to the topology of the logic. Therefore, if the system is switched on while the same input vector is applied that was forced during the power-down phase by the input circuitry, no glitches will appear. Furthermore, no logic nodes need to be charged or discharged. Consequently switching on a circuit block according to the ZigZag-scheme ensures significantly reduced power-on time.

8. SIMULATION RESULTS AND EXAMPLES

In order to verify the analytical considerations we chose two test circuits commonly used in SoC: A 5-bit carry-look-ahead adder and a 8x8-bit booth(2) multiplier. The circuits are given in Figure 3 and Figure 4, respectively.

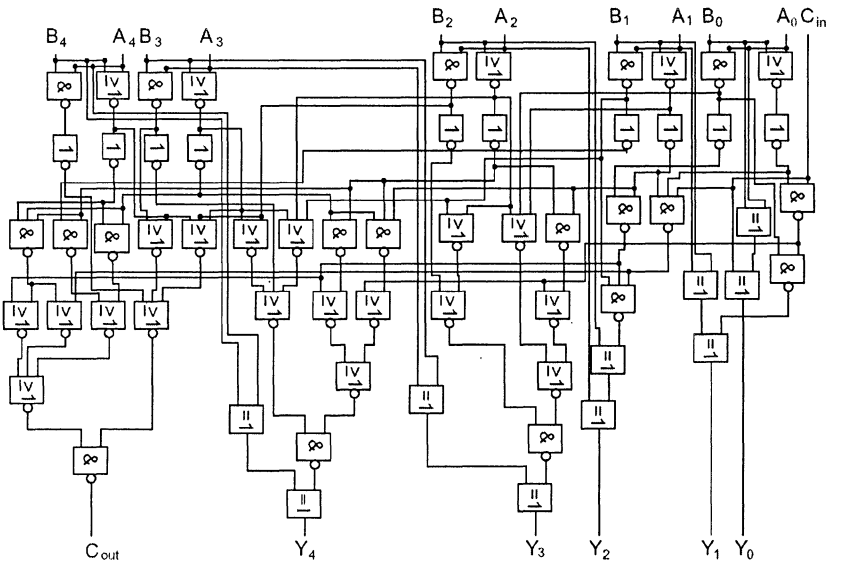

Figure 3. 5 Bit Carry Look Ahead Adder as first testbench

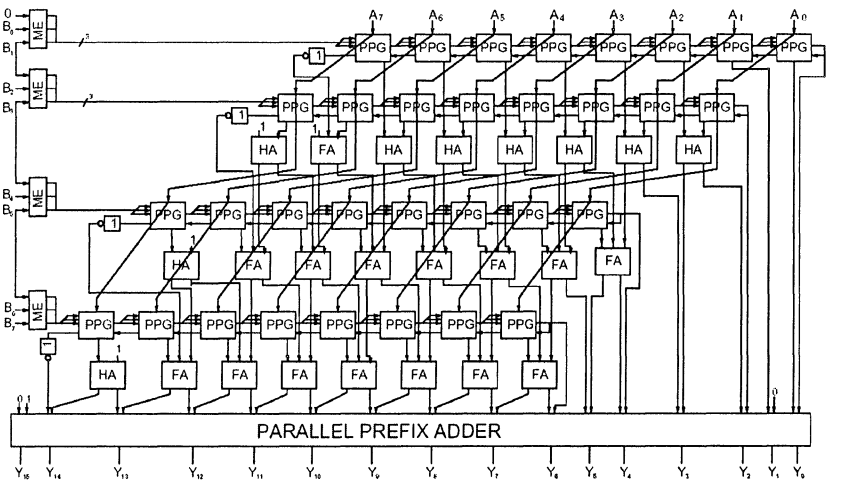

Figure 4. 8x8 Bit Booth(2) Multiplier as second testbench

We simulated both circuits assuming a gate tunneling current density of $j_T = 1.7 \cdot 10^3 \frac{pA}{\mu m}$ and a subthreshold current of $I_S' = 8.3 \frac{pA}{\mu m}$. Thus we get $\tau = 205.8$. The ratio of the logic width to the width of the switch is set to 5 in the case of the adder and 10 for the multiplier. Consequently we have to expect a degradation factor $d_{adder} = 1029$ or $d_{multiplier} = 2058$, respectively. The simulations are carried out using SPICE and BSIM 4.2 MOSFET-Model. To examine the influence of the tunneling currents the appropriate switches in the model (igcMod, igbMod) are either turned on or off.

Figure 5a shows the simulated leakage current of the adder over temperature for n-block-switching, p-block-switching and ZigZag-scheme. As expected the subthreshold current shows an exponential temperature dependence, whereas the gate tunneling current has little temperature dependence. Nevertheless in ZigZag-scheme the gate tunneling current is significantly larger than the subtreshold current even at high temperatures. In the n-block or p-block environment, leakage current varies only slightly if gate-tunneling is turned on or off. The slight difference is caused by the small tunneling current over the drain-to-gate overlap region of the switch transistor (thick gate oxide). The ZigZag implementation of the adder uses extra virtual power-rails for the first logic stage. Therefore a slight difference exists between the results in equation 11 and the simulation. For large circuits however or by using another strategy for the first stage this difference is negligible.

Fig 5b shows the simulation results for the multiplier. In ZigZag-scheme the first stage is driven by resetable flip-flops, so no extra power-rails are necessary. The subthreshold current varies exponentially over temperature and differs only slightly from total leakage in the n- or p-block switching scheme. In the ZigZag case there is a huge difference between subthreshold current of the switch and the total leakage. The strong dependence of the degradation factor d on the ratio τ of the two leakage components states that even if the gate current in BSIM was modelled inaccurately the prediction about the decreasing ZigZag benefits in future technologies would hold. Therefore, analytical examination and simulation are sufficient to derive this dependency, without a testchip manufactured in silicon.

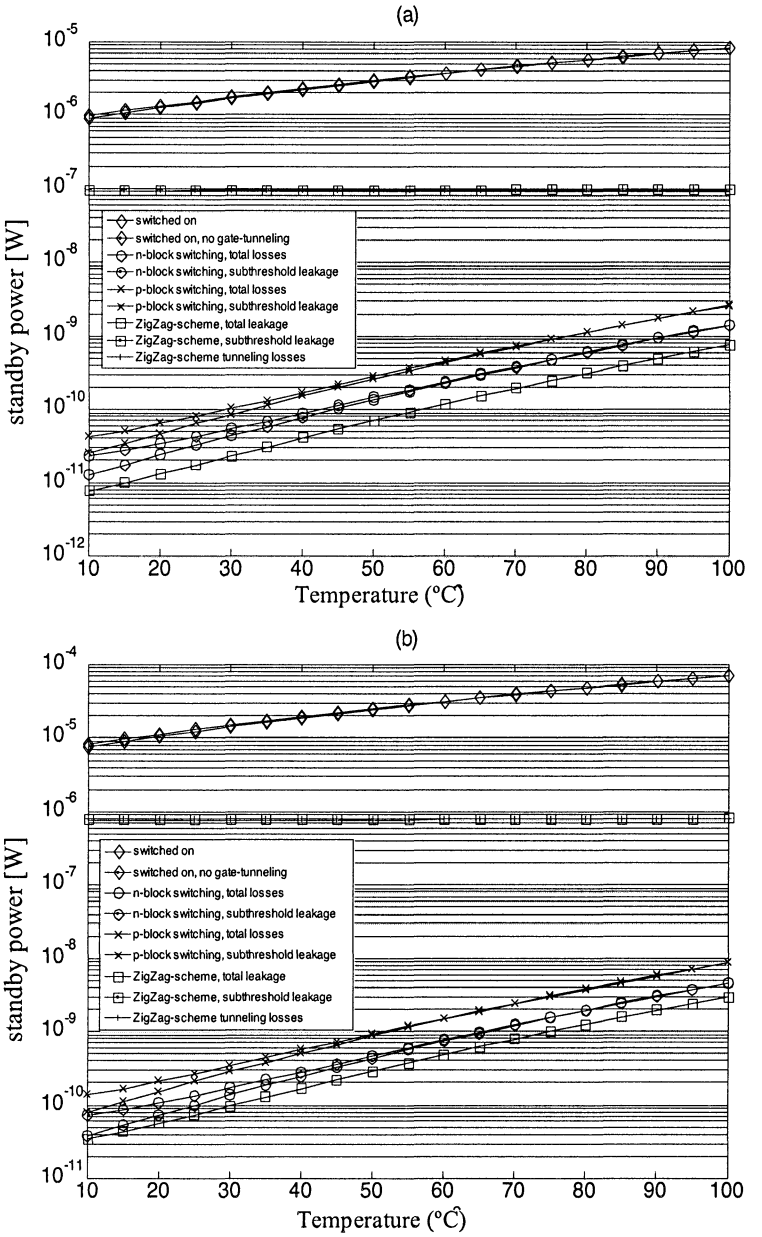

Figure 5. Leakage losses over temperature of the different cut-off schemes for the adder (upper) and the booth(2)-multiplier (lower)

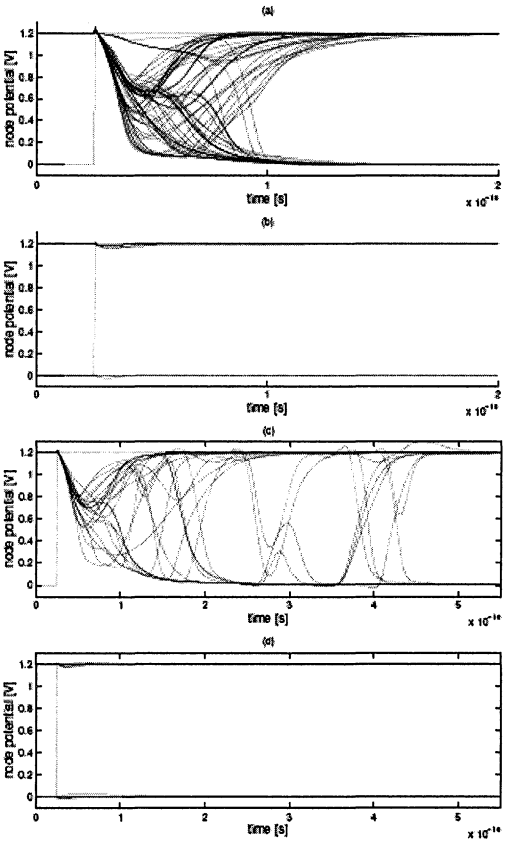

Figure 6. Behaviour of inner nodes during power-on process for ZigZag and n-block circuit block switch-off scheme: (a) adder with n-block sleep-transistor, (b) adder according to ZigZag scheme, (c) n-block switched booth multiplier, (d) multiplier according to ZigZag scheme.

Next we examined the behaviour of all signal nodes during the turn-on phase. Figure 6 a,b show the inner node potentials of the adder in the case of n-block-switching and ZigZag. As predicted, in the ZigZag case there are absolutely no glitches or switching processes, whereas in the n-block switched adder there exist many power- and time-consuming glitch activities. The multiplier has a considerably deeper logic structure. Therefore even more severe glitches have to be expected. Figure 6 c, d show some

node potentials for the two switching strategies. Again many glitches can be observed in n-block scheme and none in ZigZag-scheme. Comparing the power-on times these simulations show that the adder can be reactivated 4 times faster in ZigZag-scheme than with n-block-switching. In the case of the multiplier, ZigZag is 5 times faster.

9. COMPARISION TO RECENT WORK

As the power saving capability of ZigZag vanishes with increasing gate leakage a gate leakage suppression scheme has been proposed (GSCMOS)[12]. To suppress the gate tunneling currents an additional power switch is added to the gates assigned to the NMOS sleep-transistor in ZigZag scheme. Hence there are five power nets necessary for GSCMOS: V_{DD}, V_{SS}, two virtual V_{DD} and one virtual V_{SS} net. Therefore the place and route problem becomes even more complex than for ZigZag scheme. The outputs of all gates assigned to PMOS and NMOS switches are floating, thus there is no stack effect in the following stage and subthreshold leakage increases. The output voltage of all gates assigned only to PMOS sleep-transistor is still zero. Hence the circuit block can be reactivated rapidly without any glitches. Anyway the activation time is increased with respect to ZigZag scheme as both virtual V_{DD} nets are discharged significantly. The gates assigned to NMOS and PMOS sleep-transistors have a parasitic switch resistance both in pull-up and pull-down path. To compensate for the increased delay degradation the switches have to be upsized resulting in increased leakage currents and area consumption.

Simulations using a 90nm low-power technology show that for the same delay degradation GSCMOS does not result in increased leakage reduction ratio compared to n-block switching. Another scheme for fast block activation that results in lower design overhead and energy savings similar to n-block switching has been proposed in [13]. Glitches are avoided by turning on two distinct groups of gates with slight latency.

10. CONCLUSIONS

Two methodologies to switch-off unused circuit blocks have been examined and compared. It has been shown that ZigZag-scheme will loose more and more its leakage suppression capability if technologies with significant gate leakage are used. n- or p-block switching keeps its leakage suppression property but suffers from considerable glitches during power-up phase. Thus it depends on the application and the average power-down time

whether ZigZag or n-block switching is preferable: If there are only very short periods during which the circuit block is not needed, ZigZag will be preferable. In modern high performance technologies however the leakage suppression of this scheme is weak. If the power-down periods are long and the times of usage of the block can be estimated well, the reactivation time will be of inferior significance. Thus n- or p-block switching are the preferable schemes because of their excellent leakage supression property.

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