

A SWITCHED OPAMP BASED 10 BITS INTEGRATED ADC FOR ULTRA LOW POWER APPLICATIONS

Giuseppe Bonfini¹, Andrea S. Brogna¹, Roberto Saletti¹, Cristian Garbossa², Luca Colombini², Maurizio Bacci², Stefania Chicca² and Franco Bigongiari²

¹University of Pisa - Dipartimento di Ingegneria dell'Informazione: Elettronica, Informatica, Telecomunicazioni, Via G. Caruso 2, 56122 Pisa (Italy);

²Aurelia Microelettronica, Via Vetraia 11, 55049 Viareggio (Italy)

Abstract: *This paper describes an ultra low-power switched opamp-based integrated ADC designed using a cyclic algorithm approach, for cardiac pacemaker applications. The A/D converter shows a typical operating power consumption of 8.18 μ W for the analog part and of 9.71 μ W for the digital one, whereas the stand by dissipation is about 1 nW and 5 nW, respectively, (measured on 10 chip samples and averaged), considering a typical supply of 2.8 V. The ADC resolution is 10 b, its typical operating clock frequency is 32 kHz (sampling rate is 2.9 kSamples/s) and it is able to reach the same resolution at 2 V, with 0.7 kSamples/s sampling rate, showing a dissipation of 1 μ W for the analog part and 1.3 μ W for the digital part. Moreover, it is also characterized by low offset and no missing codes.*

Key words: Ultra Low Power, Biomedical Implantable Applications, Switched OpAmp, Analog To Digital Converter

1. INTRODUCTION

The Switched Capacitor (SC) technique needs a particular attention in the design of the switches when used at low supply voltages. In fact, the signal swing applied in these cases is dramatically reduced when a very low supply voltage is used: complementary switches and op amps do not efficiently work because of the insufficient switch overdrive¹. These problems can be solved by the use of a switched opamp (SOA) technique, instead of SC, to overcome the typical impairments of low-voltage low-power systems²⁻⁷

Please use the following format when citing this chapter:

Bonfini, Giuseppe, Brogna, Andrea, S., Saletti, Roberto, Garbossa, Cristian, Colombini, Luca, Bacci, Maurizio, Chicca, Stefania, Bigongiari, Franco, 2006, in IFIP International Federation for Information Processing, Volume 200, VLSI-SOC: From Systems to Chips, eds. Glesner, M., Reis, R., Indrusiak, L., Mooney, V., Eveking, H., (Boston: Springer), pp. 133-147.

This paper describes a switched opamp implementation of a cyclic algorithmic ADC that leads to very low power consumption. The architecture complies with the constraints of a biomedical implantable application: ultra low current consumption lower than 4 μ A, typical supply voltage of 2.8 V (even if the circuit operates properly in the supply range from 2 V to 3.5 V). Moreover, the ADC can be switched to power-off mode and wakened only when needed. The technology used is a BiCMOS 0.8 μ m, with 2 metal and 2 poly layers.

2. THE ADC ARCHITECTURE

The aim of this paper is the design of an integrated ultra-low power consumption A/D converter which operates with a standard battery supply for cardiac pacemaker applications (operating from 3.5 V down to 2 V), with a resolution of 10 bits, conversion rate higher than 2 kSamples/s, input dynamic range of 800 mV and small silicon area.

This performance has been obtained using a cyclic conversion algorithm and the SOA technique. This approach was chosen instead of others because of the following considerations. Both pipeline and sigma delta approaches could be used in applications (biomedical also) where either conversion rate or resolution are requirements more important than consumption and silicon area. In fact, the pipeline architecture is able to achieve a high conversion rate (also in low-voltage applications⁸), but it consists of a series of identical stages that consume additional power, whereas the sigma delta approach can be used in high resolution (more than 16 bits) applications, where hardware simplicity and conversion rate are not the main issues.

Instead, a successive approximation architecture (SAR) using a very low supply voltage allows one to achieve medium speed/medium resolution converter performance with a low power consumption and standard threshold CMOS devices. The results shown in the literature⁹ indicate that SAR approach is well suited for operation even below 1 V (around the threshold voltages of the device used), but the very low current dissipation ($\sim 30 \mu$ A) is achieved with a supply voltage of 1 V. In cardiac pacemaker application, a standard battery is used. It sets the supply voltage value to the typical value of 2.8 V, and thus the same value of dissipation has to be reached at a voltage value larger than 1 V. On the other hand, the SOA technique can be used in our application because of its capability of reducing the supply voltage and overcoming the limits due to the switches overdrive. In fact, the possibility of completely turning “on” opamps only in one of the two phases of the main clock, being the opamp switched off in the other phase, allows us to halve the power consumption of the entire system. This is

a great advantage, especially for systems employed in biomedical applications and particularly in pacemakers, where low-voltage and low-power requirements are mandatory.

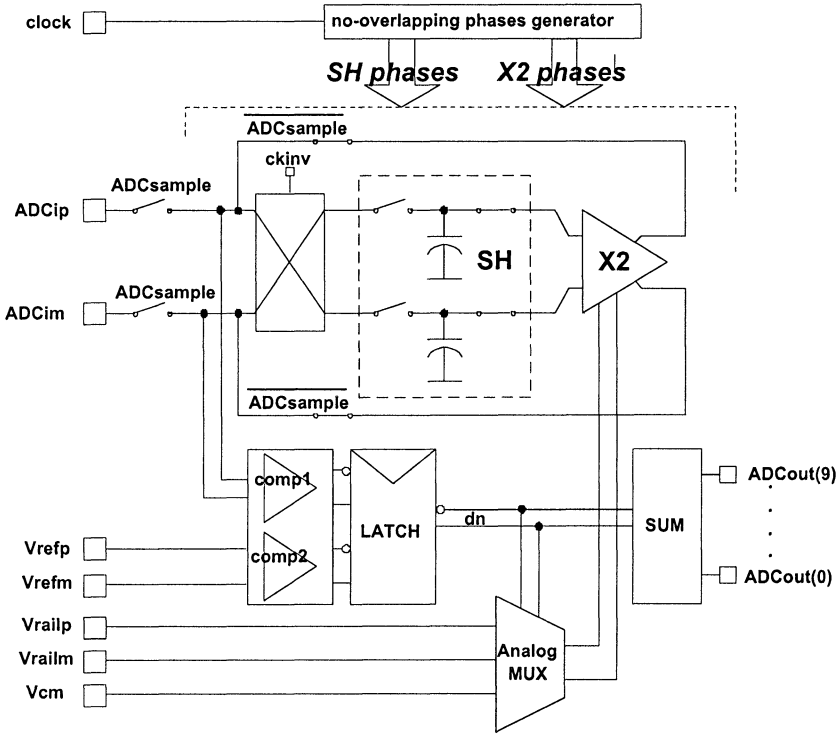


Figure 1. ADC schematic diagram

Figure 1 shows the schematic diagram of the ADC described in this paper. The architecture is a classical Cyclic/Algorithmic topology with 1.5 bit per cycle, consisting of three main blocks: a Sample and Hold (indicated with SH in Figure 1), some comparators and a Multiplying DAC (indicated with X2). The ADC works as follows:

- when *ADCsample* is asserted (see Figure 1), any analog signal present between *ADCip* and *ADCim*, that is sampled through the input switches of SH during the first phase (*phase1* in Figure 2), is converted by the two comparators (that act as a flash sub ADC) in a 2 bit digital number;
- then *ADCsample* is removed, the SH block holds the sampled signal while X2 samples the SH output. At this time the input switches are opened and a loop is created between X2 and SH.

During the following clock cycles (*phase1-phase2*), the operation continues: the SH block samples the X2 output feedback, this signal is compared by the two comparators and the X2 block multiplies by two the SH output. If necessary, a reference voltage is added or subtracted to it, according to the result of the comparison.

The ADC takes 11 clock cycles (32 kHz) to produce a 10 bits output code. A new conversion begins (and a new input analog signal is processed) when *ADCsample* becomes active again. If V_{in} is the voltage difference between the SH inputs, V_{ref} is the voltage reference ($V_{ref} = V_{railp} - V_{railm}$ which is also half of the input dynamic range of the ADC), V_{resn} is the voltage residue at X2 output of n -th conversion cycle and d_n the respective binary code, then the algorithm works as follows for each clock cycle:

$$V_{resn} = \begin{cases} 2 \cdot V_{in} - V_{ref} & \text{if } V_{in} > \frac{V_{ref}}{4} & d_n = 10 \\ 2 \cdot V_{in} & \text{if } -\frac{V_{ref}}{4} \leq V_{in} \leq \frac{V_{ref}}{4} & d_n = 01 \\ 2 \cdot V_{in} + V_{ref} & \text{if } V_{in} < -\frac{V_{ref}}{4} & d_n = 00 \end{cases}$$

The digital result d_n is the input of the block SUM that encodes the output.

The SOA technique, traditionally used to reduce the operating supply voltage⁸, is mainly used in this case to achieve a reduced power consumption, for a 2 V minimum supply: in fact, if SH is “on”, X2 is “off” and vice versa. When a block is off, the SOA output stage is in high impedance and is pulled to V_{cm} (common mode voltage of the ADC) by the related switches.

Figure 2 shows the SH architecture employed in this design. It consists of switches (in a transmission gate configuration), a SOA, two sample capacitors C , two hold capacitors C (of the same value) and two capacitors having a value of $C/8$, that avoid large spikes on the virtual ground to be traded off with the offset that these capacitors produce.

When *phase1* is low (sample phase), the charge is stored on the sampling capacitors C and SOA output stage is in high impedance. In order to minimize the delay caused by the slew rate, that can be high in low-power applications, SOA output stage is pulled to the middle of the dynamic output

range (V_{cm}) in this phase. When *phase1* is high, the inputs of this stage are pulled to V_{cm} (while the output of the X2 stage is pulled to V_{cm}), then SOA is turned “on” and all the switches are turned “off”. As a consequence, the charge is stored on the sampling capacitors of the X2 stage.

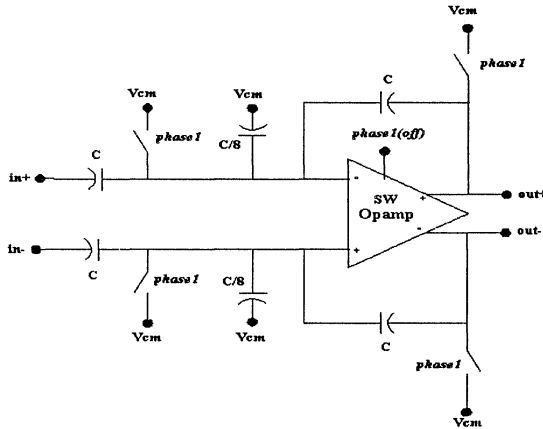


Figure 2. Sample and Hold (SH) detail

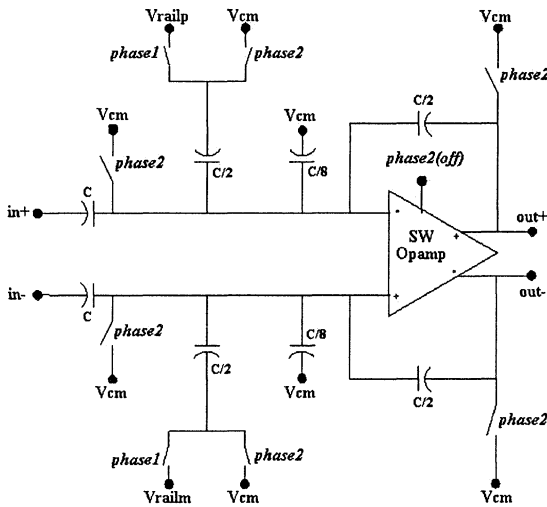


Figure 3. Multiply by two (X2) detail

Figure 3 shows the X2 architecture. There are two capacitors with the same value of the hold capacitors ($C/2$), in order to obtain a 1.5 bits

requirement. During *phase2*, the charge is stored “on” the sampling capacitors (through the hold phase of the SH stage), $C/2$ input capacitors are pulled to V_{cm} (as in the output stage of the SOA). At the end of *phase2*, the amplifier is turned “on”. During the following phase (*phase1*), the $C/2$ input capacitors are pulled to one of the V_{rail} voltages, depending on the result of the $\pm V_{ref}/4$ comparison. In this way, the subtractions or additions described before are executed. It is worth noting that the 0.5 bits redundancy is obtained using only two non-overlapping phases (*phase1-phase2*) and the complementary ones (since all the switches are implemented as transmission gates).

2.1 Switched Opamp

The amplifier employed in the ADC analog core is a simple 2 stages Miller compensated OTA (Figure 4). The amplifier has a fully differential architecture, mainly to improve power supply rejection ratio (PSRR) and to enhance the signal swing. It also has an active Common Mode FeedBack circuit (CMFB).

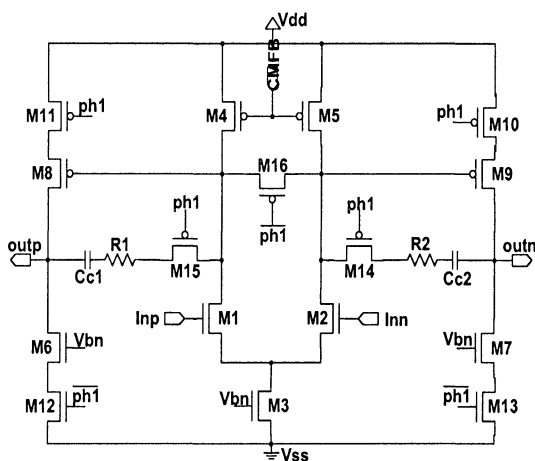


Figure 4. Fully differential opamp implementation

During the opamp inactive phase, the output branches are turned off and the input stage is kept “alive” to guarantee a fast turn on of the amplifier. The dissipation is 150 nA for the input stage and 1 μ A for the output stage (500 nA per branch). This means that the current consumption, excluding CMFB circuit, is 1.15 μ A during on phase and 150 nA during off phase.

A special attention was paid in designing M4 and M5 in strong inversion (as they work as current mirrors), and the input pair M1, M2 in weak inversion, designing the OTA with suitable dimensions and layout in order to reduce the offset. Switches M14 and M15 prevent the discharge of the compensation capacitors during the off phase of the opamp, thus allowing a fast recovery. Moreover, a switch (M16) between the drains of the input transistors shorts them during the inactive phase, so avoiding the saturation of the input stage caused by the absence of feedback.

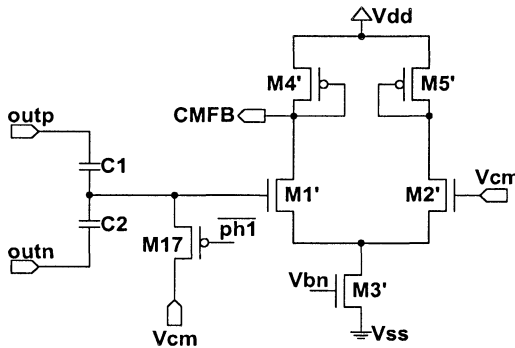


Figure 5. Common Mode FeedBack circuit

The fully differential opamp needs a CMFB (Figure 5) to work properly. A switched capacitor approach was chosen, due to its simplicity and the high linearity it can give.

The outputs are averaged by C1 and C2 during on phase; this averaged voltage is the input of a simple opamp (replica of the input stage of the main amplifier) and is compared to the wanted Common Mode Voltage (V_{cm}). A feedback signal is generated (CMFB) that controls the current of the input stage of the main opamp (see Figure 4).

Table 1. Opamp simulation results

Parameter	Value	Unit
Supply Voltage	2 ÷ 3.5	V
Supply Current	1.305	μA
Temperature	-15 ÷ 45	°C
Open Loop Gain (A _o)	101	dB
Gain Bandwidth Product (GBW)	387	kHz
Phase Margin (PM)	60	°
Slew Rate (SR)	0.12	V/μs
Silicon Area	0.081	mm ²

During the off phase, capacitors $C1$ and $C2$ are reset ($outp$ and $outn$ are put to V_{cm}) through switch $M17$ and the CMFB is kept “on”, to be ready for the next phase.

Table 1 summarises the main performance obtained during the simulation of the entire opamp with a load of 4 pF. As shown, the gain is very high (more than what is needed to reach the required linearity) because of the two stages architecture. It is worth noting that slew rate requirements are heavily reduced in this application, thanks to the fact that the output stages are pulled to V_{cm} during the inactive phase.

2.2 Comparators

In order to produce a 0.5 bits redundancy, two comparators have been used in this design. It is important to note that a 1 bit per cycle architecture needs only one comparator, but it is not possible to relax the offset requirement, and the technique described in the next Section does not produce those advantages in terms of integral and differential non-linearity. An Input Offset Storage (IOS) method is used in this design, in which closing a unity gain loop around the preamplifier and storing the offset on the input coupling capacitors performs the offset cancellation¹⁰.

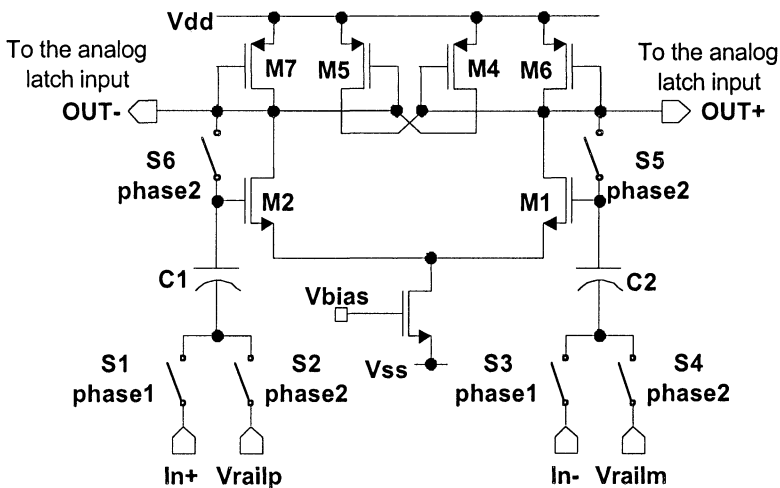


Figure 6. Schematic diagram of the preamplifier

The circuit schematic is shown in Figure 6. During *phase2*, a reference voltage is applied to the inputs of the preamplifier and the offset is stored on the capacitors $C1$ - $C2$. Instead, the input signals (coming from SH inputs) are

applied and the outputs fed the inputs of the cascaded analog latch stage, during *phase1*. The value of the capacitors *C1-C2* is 600 fF, so that the kT/C noise contribution is about 85 μ V: a value lower than LSB value (about 780 μ V). The power consumption of this stage is 180 nA in the typical case (2.8 V power supply, 2.9 kS/S) and about 50 nA in the “minimum” case (2 V power supply, 0.7 kS/s).

2.3 Offset reduction in the amplifiers

In both SH and X2 blocks, the autozero operation of the amplifier allowed in classical SC architectures cannot occur because in the sample phase (*phase1* for SH for instance) SOA output is “off”, so, this effect results in a huge loss of codes and potential linearity problems.

However, in the second clock cycle (the first after *ADCsample* is on), the SH inputs are inverted, through the signal clock *ckinv*. At the third clock cycle *ckinv* (Figure 1) turns “off” and normal conditions are restored. So, the offset stored the first time, that at the end of conversion is multiplied with 2^{N-1} (N = number of bits of the ADC), is subtracted with next offsets (next clock cycles) that are multiplied with 2^{N-k} , where $k = 2..10$ is the number of the clock cycle. This also means that, after *ADCsample* is on, the residual signal of conversion is inverted: the SUM block thus needs additional logic⁸.

2.4 2.4. ADC timing diagram

The reset signal asynchronously initialises the digital section of the ADC: the output register is loaded to “0” as conversion result, but *ADCdav* is low so this is not considered a valid result. An initialisation is recommended each time a new data acquisition begins, but the reset pulse width must be as short as possible to minimise power supply consumption.

The ADC timing diagram is shown in Figure 7: the acquisition mode is “free running” and the data stream is collected by a microcontroller which can operate in edge mode or level mode. In fact, *ADCdav* raises each time that a valid data conversion is available (edge triggered) and remains stable until the ending of a new conversion (level triggered). The “one shot” acquisition mode is a trivial sub case.

The ADC starts when it wakes up from stand-by condition. The internal state is bounded to rising edge of the clock; an initial start up time allows the analogue part to reach a steady state and then the conversion starts (the internal signal *ADCsample* is shown for clarity) on the clock falling edge.

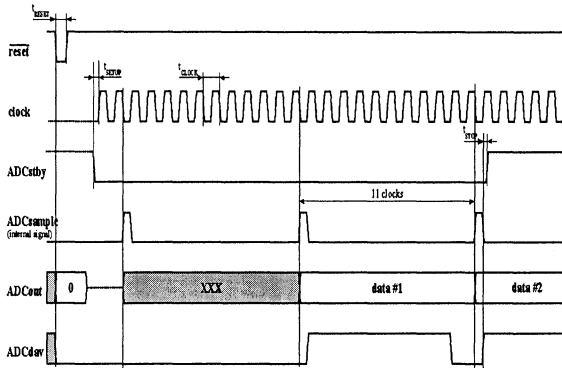


Figure 7. ADC timing diagram

To process the input value, the ADC takes 10 clocks plus an additional clock to reinitialise the internal logic. The data output $ADCout$ [9:0] is registered, so the data are stable until the register is updated.

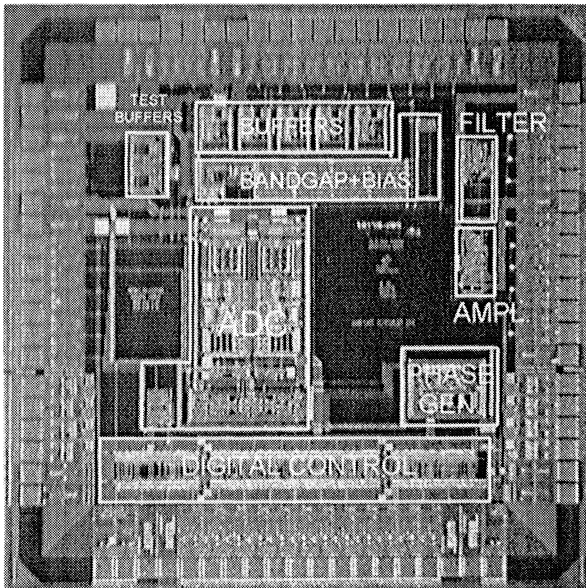


Figure 8. Chip microphotograph (die area about 9 mm^2)

3. EXPERIMENTAL RESULTS

The A/D integrated converter was fabricated in a 0.8 μ m BiCMOS technology with 2 metal and 2 poly layers. The ADC described in the previous Section has been designed as a part of a prototype chip developed for implantable pacemakers (the chip microphotograph is shown in Figure 8). The front end section consists of an input amplifier with AC coupling - externally provided - to avoid input offset amplification, a low pass filter, and the 10 bits ADC.

The prototype includes a bandgap voltage reference, which is referred to ground, five voltage buffers to provide the proper references for the ADC and the other devices.

Table 2. Measurement conditions

Power consumption	Supply Voltage [V]	Clock Rate [kHz]	Bias Current
Maximum	3.5	32	full
Typical	2.8	32	full
Minimum	2.0	8	full

The chip is pad limited and the prototype silicon area could have been reduced (see Figure 8), if no test pads were used. In fact, the ADC cell area is about 0.8 mm². Table 2 shows the operating conditions of the A/D converter. Nevertheless, all the prototypes have been characterised with different combinations of power supply, clock rate and bias current, showing a proper functionality in every condition.

Table 3. Summary of the ADC performances

	Minimum Power Consumption	Typical Power Consumption	Maximum Power Consumption	Unit
Resolution	10	10	10	bit
Consumption (analog)	0.56	2.92	3.90	μ A
Consumption (digital)	0.67	3.47	4.17	μ A
INL	1.13	0.98	0.85	LSB
DNL	0.73	0.67	0.75	LSB
Input Noise	0.43	0.42	0.40	mV (RMS)
Offset	0.72	0.73	0.70	mV
THD	56.6	56.3	57.6	dB
SFDR	60.2	59.6	61.1	dB
ENOB	8.4	8.4	8.4	bit
Offset drift	-	21.4	-	μ V/ $^{\circ}$ C
Gain drift	-	100	-	ppm/ $^{\circ}$ C
Active Area		0.8		mm ²
Technology	AMS 0.8 μ m BiCMOS			

Very low power consumption has been measured for the analog core when reduced power supply, clock rate and bias current were used: 0.56 μ A in the minimum case. Digital core dissipation (see Table 3) is rather high for the target application (total consumption exceeds 4 μ A in typical case), but no particular attention has been paid to this point, because of the following considerations:

- in implantable device applications, an embedded processor that can implement the main part of the digital section of the ADC is commonly available.
- no low power digital library was available for the considered technology, so a standard digital library was used.

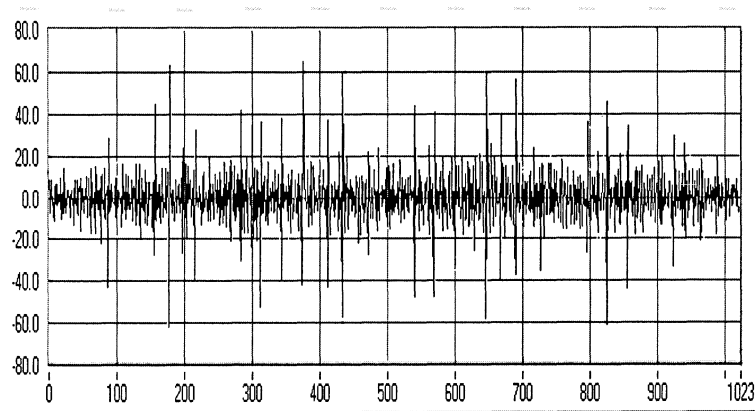


Figure 9. Measured DNL (LSB*100) in typical conditions

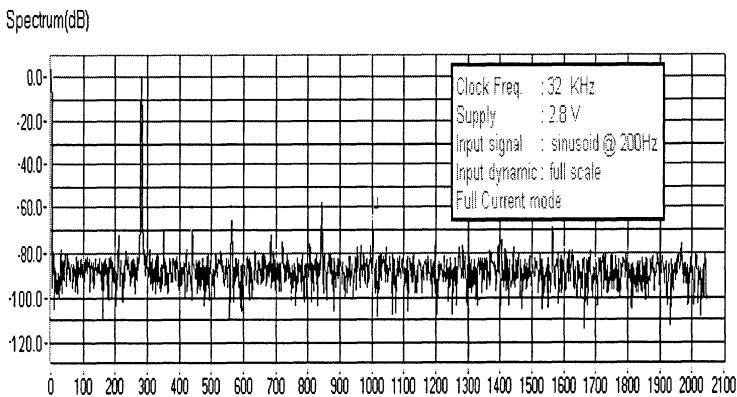


Figure 10. Output spectrum for an input tone at 200 Hz

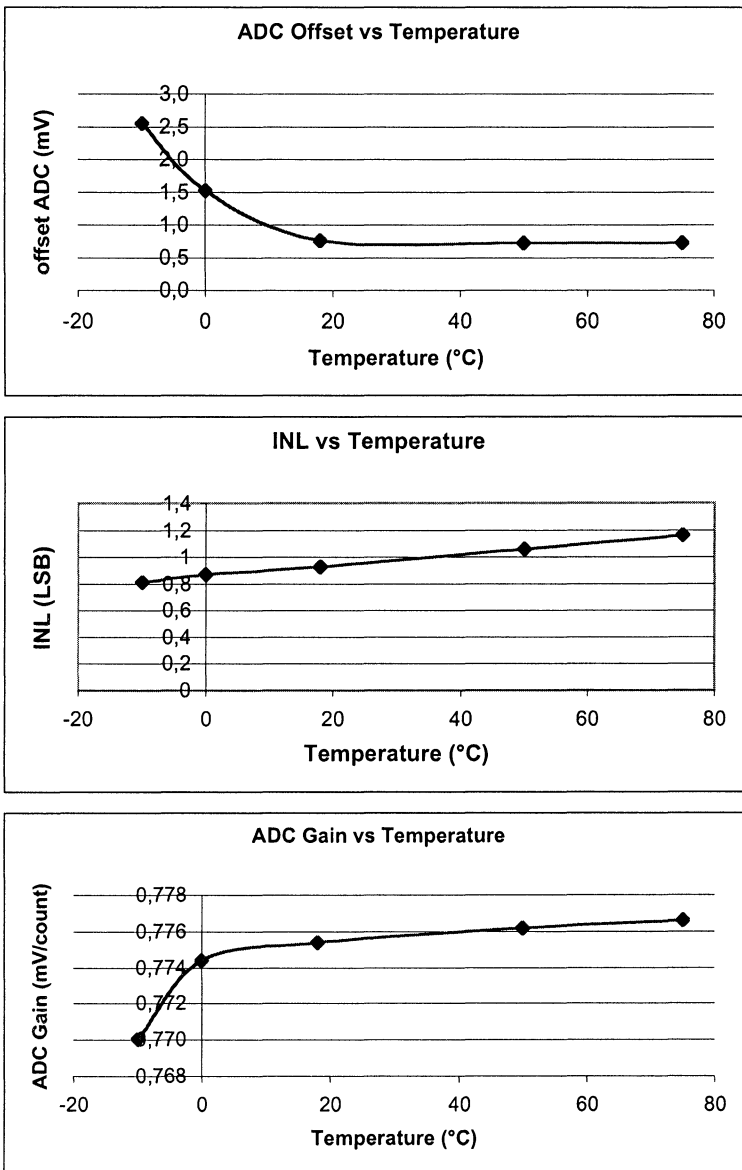


Figure 11. Offset, INL and Gain versus Temperature

The measured differential non-linearity (DNL) curve (typical case) and the measured output spectrum (2048 point FFT spaced 1.42 Hz each other) of a reconstructed 200 Hz full scale sine wave sampled at 2.9 kS/s with a supply voltage of 2.8 V are shown in Figure 9 and Figure 10, respectively.

The maximum value of the measured DNL is approximately of 0.7 LSB (see also Table 3). The main measurement results are summarized in Table 3.

The measured offset, integral non-linearity (INL) and gain as a function of the temperature (in the range $-10/+75^{\circ}\text{C}$), in typical case, are shown in Figure 11. It can be noticed that the functionality of the ADC is guaranteed in a wide range of temperature.

4. CONCLUSIONS

Implantable biomedical devices are asked to operate for long time with long life batteries (with a duration of at least 6 years) and the resolution of the sensing channel is going to increase (over 8 bits). Most of the existing ultra low-power ADCs does not provide a resolution as high as 10 bits.

In this paper we have shown how the SOA technique can be used to achieve 10 bits resolution for an ADC to be used in a cardiac pacemaker characterized by an ultra low power consumption, a low die area and the cyclic conversion algorithm approach.

Moreover, the measurements carried out on the ADC prototypes demonstrate the full functionality of it with no missing codes, with a consumption of 1.23 μA , 0.7 kS/s sampling rate and 2 V supply voltage.

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