

Precisely assembled Multi Deflection Arrays – key components for Multi Shaped Beam lithography

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Abstract

Multi shaped beam lithography requires the precise and durable alignment and fixation of MEMS based Multi Deflection Arrays on stable ceramic system platforms using vacuum and high temperature compatible interconnection and joining technologies. Micron accuracy during assembly is accomplished by mark detection using image processing and 3DOF alignment procedures; while interconnection as well as precise fixation is carried out using a fine pitch solder bumping process. Qualification investigations using electron beam equipment show that the precisely aligned multi shaped beam arrays are able to deflect the electron beams in accordance with the simulation results.

Introduction

Multi Shaped Beam Lithography (MSB) is a promising approach for high throughput mask and direct writing that addresses the shot count/writing time bottleneck [1], [2] for the 22 nm node and beyond. Multiple apertures and electrodes necessary for a beam deflection can be manufactured by new developed MEMS micromachining technologies. Nevertheless, for integration into the electron beam column a hybrid assembly of several MEMS Multi Deflection Arrays (MDA) with an aperture overlaying accuracy of less than 1 μm , thermal stability up to 100 $^{\circ}\text{C}$ and low out gassing rates must be accomplished. The development of the whole process chain of manufacturing, assembly and integration was necessary for realization of a new lithography tool for MSB.

Multi Deflection Array – assembly requirements

The x- and y deflection functionality of a Multi-Beam Deflector (MBD) requires the face to face alignment and mounting of two individual deflection arrays that deflect the beam either in the x- or y-direction only. Figure 1 shows the beam forming and deflection principle used in Vertical shaped beam (VSB) and Multi shaped beam (MSB) lithography. Between the two arrays a small distance is desired in order to keep deflection aberrations low. Due to this for the implemented assembly it was chosen to mount each MDA chip on an individual LTCC carrier and afterwards align these sub-assemblies with respect to each other. The alignment has to be done in the x- and y- direction with less than 1 μm accuracy. Tip (Rx) and tilt (Ry) degrees of

freedom are given by the contact of the LTCC carriers; the rotation around z (R_z) has to be aligned with an accuracy of less than 17 mrad. Because of the MBD operation in an electron beam environment under vacuum conditions the used materials have to be non magnetic, radiation resistant and vacuum suitable with low outgassing rates. To maintain the cleanliness of the apertures of the MDA chip the assembly has to take place under clean room conditions (class 5 ISO 14644-1). A temperature stability of the assembly device of < 1 K is necessary to reach the high alignment accuracy and measurement uncertainty.

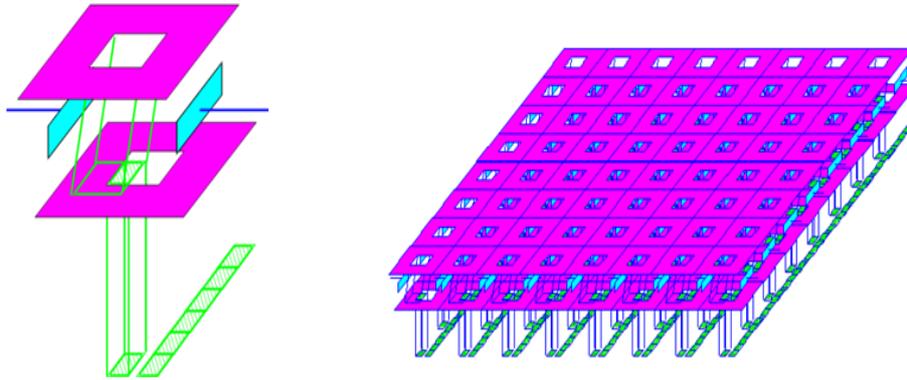


Figure 1: Schematic comparison of VSB (left) and MSB (right) exposure principle

Multiple apertures and electrodes MEMS technology

In MEMS surface micromachining technology based on thick poly silicon layers is a common method for the fabrication of sensors and actuators. This technology has been developed for production of MEMS gyros and MEMS accelerometers with a layer thickness of about 11 μm . Fraunhofer ISIT established this kind of process named PSM-X2 [3] during the last years supporting automotive sensor production. Using this technology, enhancing EpiPoly thickness up to 85 μm with an aspect ratio >10 for the deflectors and combining it with double layer Buried Poly wirings Multi Deflection Arrays (MDA) within specifications for multi shape beam writing application were manufactured. A cross section of this modified PSM-X2 process is drawn in fig. 2. The challenge of precise electrode shaping for accurate deflection control and low resistivity wiring for small time constants for beam deflection could be fulfilled. Figure 3 shows 65 μm high, well shaped deflection electrodes close to the aperture opening for the electron beam. Additional alignment marks are structured during the aperture etching process to guarantee lithographic accuracy of the mark positions with respect to the beam apertures. These precise marks will be used for the assembly process.

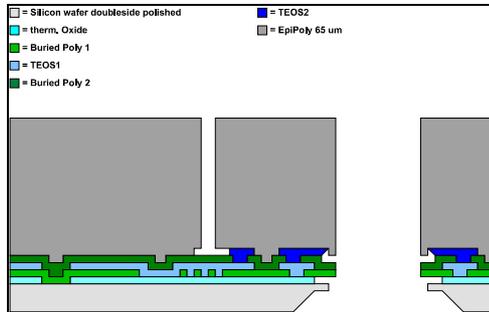


Figure 2: Cross section of a poly silicon MDA

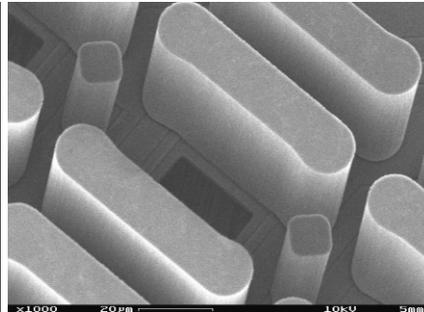


Figure 3: SEM closeup of a 4x4 MDA chip (poly silicon layer 65μm thick)

LTCC carrier system platform

The carrier system platform, a multi layer printed circuit board, is made of “Low Temperature Cofired Ceramics” (LTCC). Within this carrier cavities and geometrical structures are located for passive pre alignment of the MDA chip. Screen printed wirings provide signal routing and localized land patterns for contacting the MDA chip by soldering, furthermore even passive components such as thermistors and sensors could be integrated. The LTCC carrier provides a thermally stable system platform that’s CTE is matched to the silicon based MDA and has a close to zero out gassing rate for usage in the electron optical column (EOC) (see fig. 4).

The design of the LTCC carriers consists of seven layers of LTCC tape, using three layers with 90 μm thickness and four layers with 200 μm thickness for increased mechanical strength. The design utilizing screen printed thick film metallization comprises two outer contacting layers, two inner routing layers and two internal shielding layers. Additional thin film metallization of the outer layers prevent electric charging of the assembly in the EOC.

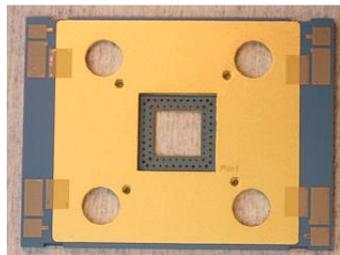


Figure 4: LTCC carrier

Layer stack details:

- Contacting and bonding layer, 90 μm
- Routing layer, 90 μm
- Routing and shielding layer, 90 μm
- Mechanical support layer, 200 μm
- Mechanical support layer, 200 μm
- Shielding layer, 200 μm
- Outer contacting layer, 200 μm

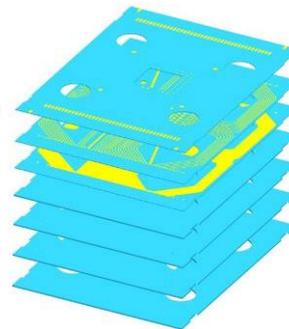


Figure 5: schematics of the LTCC carrier layer stack

Solder bumping fixation technology

A fine pitch Solderjet Bumping technology was applied for fixation and contacting of the MDA with respect to the LTCC carrier and second for the fixation of two carriers after alignment. Solderjet Bumping is a flux free laser-based soldering process that places bumps of a wide

variety of soft solder alloys, e.g. tin-based lead free solders or eutectic gold-tin (Au80Sn20) onto different substrates, such as flip chip or MEMS/MOEMS devices. It allows the hybrid integration of micro-optical and micro-mechanical components on smart system platforms and provides localized and time restricted energy input, minimizing potential damage to the components. The solder bumping device integrates the process steps of handling of the spherical solder preforms with a diameter ranging from 80 μm to 760 μm , the reflow and the application of the solder to the joining geometry, thus increasing repeatability and enabling for a high degree of automation [4], [5], [6].

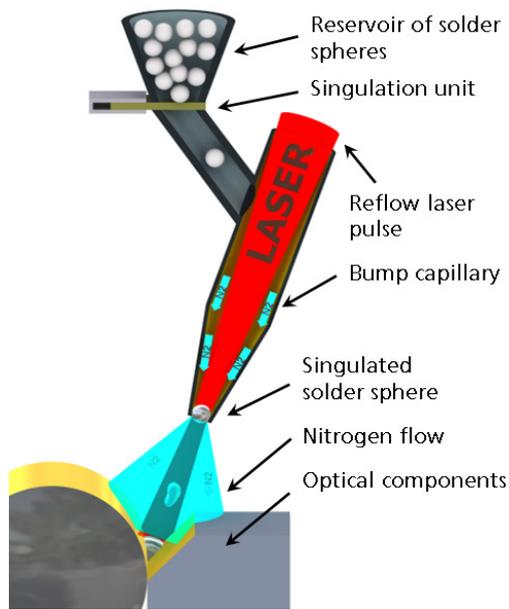


Figure 6: Simplified schematics of the solder bumping bond head



Figure 7: bond head in assembly environment

The basic principle of solder bumping is shown in figure 6. Spherical solder preforms get singularized and transferred from a reservoir to the placement capillary that has an inner tip diameter which is conical at the end and is slightly smaller than the diameter of the solder spheres. Next to the joining area a laser pulse heats and melts the solder sphere and the nitrogen pushes the solder volume out of the capillary accelerating it towards the components to be joined. The liquid solder hits the wetting surfaces and forms the solder joint by partially transferring its stored thermal energy to the substrate and component to be joined and creating the intermetallic phases during re-solidification. Solder Spreading and re-solidification takes about 10 ms and is mainly influenced by the thermal conductivity of the joined materials. The solder joints provide mechanical fixation of the components as well as a good thermal and electrical connectivity between the MDA chip and the LTCC carrier. Furthermore the joints provide a good long term, thermal and radiation stability and humidity resistance during usage in the EOC. Most promising for the MBD assembly is that the de-alignment during solder bumping fixation can be minimized to less than 1 μm [5]. Ultimate shear forces of up to 17 N were achieved by soldering optical components to LTCC and alumina platforms using two 400 μm solder spheres with a dominant failure mode of rupture of the glass component [6]. The shear strength of the solder joints can easily exceed the bulk material strength of typical materials in photonic packaging.

Assembly of the MBD

The assembly of an MBD can be divided into two assembly steps. First, a MDA chip is aligned and fixed to the LTCC system carrier. During this assembly step the alignment criteria is the positioning of the MDA contact pads with respect to the contact via holes of the LTCC carrier, requiring an alignment accuracy in the range of 10 μm to 20 μm . This requirement results from the necessity of the mechanical and electrical contact of the MDA chip and the LTCC carrier. The MDA chip is placed at a fixed position by the first gripper of the assembly device (fig. 8). The LTCC carrier then gets positioned by an additional gripper, which can be moved in the x-, y- and Rz direction for the alignment of the LTCC carrier to the fixed MDA chip. In the next assembly step the LTCC carrier is placed onto the fixed MDA chip by the assembly device. The initial position for the alignment process of the LTCC carrier with respect to the MDA chip is the planar contact of the upper surface of the MDA chip and the lower surface of the LTCC carrier. The pressing force given by the planar contact of the LTCC carrier and the MDA chip should be less than 1 N and is realized by a flat spring within the assembly device that can balance the tip and tilt mismatch between LTCC carrier and MDA chip. The contact pads of the MDA chip are detected by a microscope equipped with a reflected light illumination and a CCD imaging camera, focusing the pads through the vias of the LTCC carrier (fig. 9). During the alignment process the position of the contact pads are detected by an image processing algorithm. If all 76 contact pads of the MDA chip are positioned within the centre of their respective via hole in the LTCC carrier the MDA chip can be fixed to the LTCC carrier by solder bumping AuSn spheres with a diameter of 200 μm into the holes. All solder joints of the MDA chips fixed to the LTCC carriers have to be inspected by an optical and electrical inspection before they subsequent assembly.



Figure 8: Assembly device

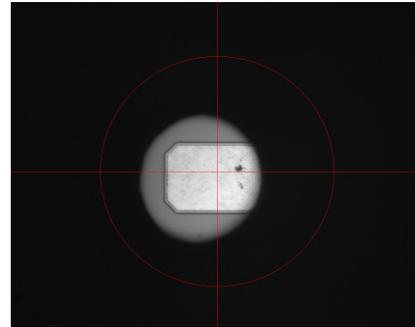


Figure 9: MDA contact pad inside a via hole of the LTCC carrier

The solder joints provide both mechanical fixation and electrical contacts with a resistance of less than 1.5 Ω per contact. Thermal cycling up to 80 $^{\circ}\text{C}$ peak temperature shows no significant change in electrical behavior. Shear force measurements show an average ultimate strength of 10.5 N per solder joint. The principal failure mode during testing is the disruption of the LTCC rather than the breakup of the solder alloy.

In the second assembly and alignment step, two LTCC/MDA sub-assemblies are aligned and mounted with respect to each other. For this assembly task lithographically structured alignment marks within the MDA chip are used for alignment. An overlay accuracy of better than 1 μm has to be reached to guarantee the performance of the MSB device, including the whole error budget of alignment and mounting.

The device for the assembly of the two LTCC/ MDA sub-assemblies is similar to that for the first assembly step. The lower LTCC carrier is fixed within the assembly device by a first gripper; the upper LTCC carrier is handled by an adjustable gripper. The LTCC carriers are put together face to face with mechanical contact of the LTCC carriers. The electrode structures of the MDA chip are protected by the lowered design of the MDA chip support of the LTCC carrier.

An assembly procedure starts with the detection of the alignment marks of the lower MDA chip. Overall eight alignment marks are detected, their centre of gravity being calculated and saved with respect to the field of view and the position of the x-y-positioning system for later calculation of the alignment status. After the detection of the alignment marks of the lower MDA chip the upper MDA chip gets positioned in the assembly device. In this status of assembly the alignment marks of the lower MDA chip are masked by the upper MDA chip. To check the position of the lower MDA chip with respect to the upper MDA chip during the assembly two additional alignment marks are used. These alignment marks are designed having two larger apertures allowing the detection of two reference marks of the lower MDA chip looking through the marks of the upper MDA chip. By this the position of the two MDA chips compared to each other can be calculated and any movement of the lower LTCC carrier during the alignment process can be compensated. The alignment position of the upper alignment marks is also measured by mark detection and image processing. The alignment status of the upper MDA chip with respect to the lower chip then can be calculated by comparing the lower and the upper mask position. After the calculation the upper LTCC carrier is aligned to the calculated position. The alignment process iterates until the position failure is less than 500 nm. The control of the assembly process is implemented by use of the Software LabView® combining the control of the positioning system, the image processing and the calculation algorithms (see fig. 10).

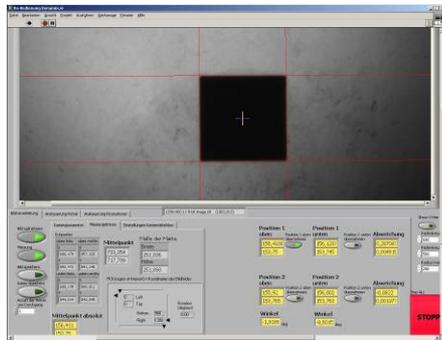


Figure 10: Alignment control user interface

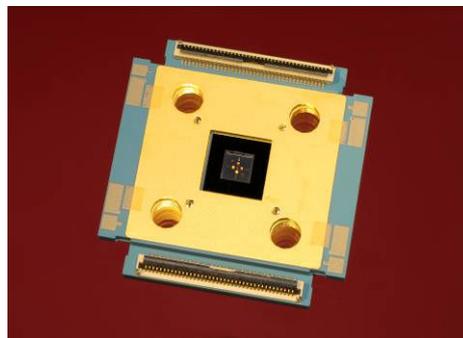


Figure 11: MBD assembly

For the evaluation of the assembly process the alignment positions of all assembly steps are detected and saved, enabling for a deviation evaluation of the MBD assembly during the fixation by solder bumping. The measured misalignment of the MBD assemblies is less than $1 \mu\text{m}$ (see fig. 12), dependant from the x- and y-direction.

The alignment status was detected and calculated for each of the four alignment marks. Before soldering it exhibits a maximum error of 500 nm with respect to the target position of the first integrated MDA chip. After soldering a misalignment of about 100 nm to 500 nm in x-direction was calculated. In y-direction a misalignment of 200 nm to 600 nm in y-direction was calculated. The difference of the misalignments of the different alignment marks positions depends on the measurement uncertainty during the mark detection because of the different quality of the alignment marks. During further evaluations using a redesigned LTCC carrier

and optimized alignment marks an overlap accuracy of about 300 nm at MBD assemblies #6 to #8 was reached.

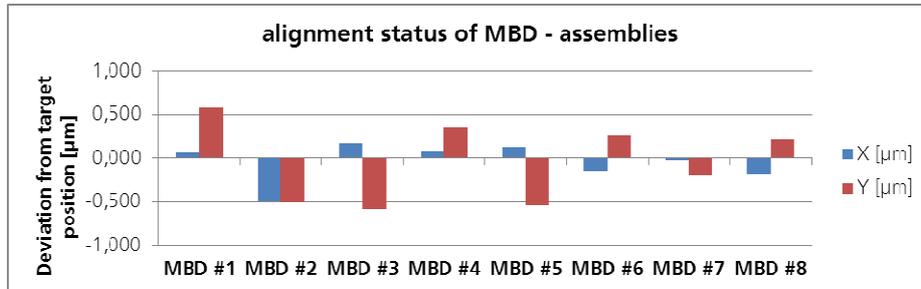
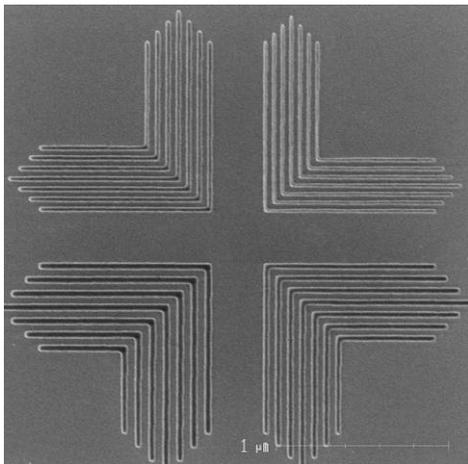


Figure 12: alignment status of MBD assemblies in x- and y-direction

Summary

The developed LTCC carrier platform is the basic component for the integration of the MDA chip. The solder bumping technology has been successfully used for the MDA assembly and alignment process during MBD manufacturing. An assembly accuracy of less than 1 μm was reached during the whole process chain of MBD manufacturing.

The manufacturing and evaluation of several prototypes of MBDs prove an overlay accuracy of 1 μm . The functionality of beam deflection using these assemblies was demonstrated by VISTEC Electron Beam GmbH. Figure 13 shows resolution test structures which have been exposed with the MSB 3050 test tool on silicon. The used resist is HSQ XR1541 (Dow Corning) at a thickness of 40 nm. As can be seen, lines down to a resolution of 25 nm can be well resolved using existing variable shaped beam electron optics with integrated MSB deflection arrays.



The promising deduction of this result is, that MSB is both well aligned with the resolution enhancement potential of variable shaped beam electron optics and flexible in that respect concerning future technology nodes.

The next steps in MBD assembly activities will be the further automation of the assembly and alignment processes for higher efficiency of manufacturing.

Figure 13: Resist image of resolution test pattern (1:1 lines and spaces) exposed with the MSB 3050 test tool in HSQ resist on silicon wafer: lower left 40 nm, lower right 35 nm, upper left 30 nm, upper right 25 nm line width.

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